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Mechanical Data

LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

D1312, SEPTEMBER 1973-REVISED MARCH 1988

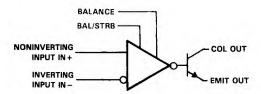
- Fast Response Times
- Strobe Capability
- Designed to be Interchangeable with National Semiconductor LM111, LM211, and LM311
- Maximum Input Bias Current . . . 300 nA
- Maximum Input Offset Current . . . 70 nA
- Can Operate from Single 5-V Supply

description

The LM111, LM211, and LM311 are single highspeed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, VCC+ or VCC-. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$. The LM211 is characterized for operation from $-25\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$, and the LM311 is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

functional block diagram



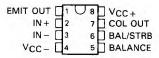
LM111 ... J PACKAGE (TOP VIEW) NC 1 1 1 NC EMIT OUT 2 13 NC IN+ 3 12 NC IN- 4 11 VCC+ NC 5 10 NC VCC- 6 9 COL OUT

LM111 . . . JG PACKAGE LM211, LM311 . . . D, JG, OR P PACKAGE (TOP VIEW)

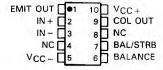
8

BAL/STRB

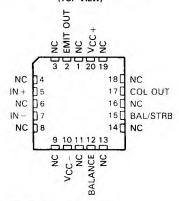
BALANCE [



LM111 . . . U FLAT PACKAGE (TOP VIEW)



LM111 . . . FK CHIP CARRIER PACKAGE (TOP VIEW)



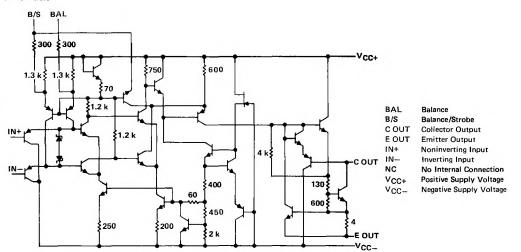
NC-No internal connection

AVAILABLE OPTIONS

OPERATING	VIO MAX			PACK	AGE		
TEMPERATURE	AT 2500	D SMALL	FK CERAMIC	J CERAMIL	JG CERAMIC	P PLASTIC	U
RANGE	TA - 25°C	OUTLINE	CHIP CARRIER	DIP	DIP	DIP	FLATPACK
-55°C to 125°C	3 mV		LM11":-	LM111J			LM111U
-40°C to 85°C	3 mV	LM211D			LM211JG	LM211P	
0°C to 70°C	7.5 mV	LM311D			LM311JG	LM311P	

The D package is available in tape and reel. Add an R suffix when ordering, e.g., LM311DR.

schematic



Resistor values shown are nominal and in ohms.

LM111, LM211, LM311 DIFFERENTIAL COMPARATORS WITH STROBES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM111	LM211	LM311	UNIT
Supply voltage, V _{CC+} (see Note 1)	18	18	18	٧
i: ly voltage, V _{CC} (see Note 1)	- 18	- 18	18	٧
uniterential input voltage (see Note 2)	±30	±30	±30	٧
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	٧
Voltage from emitter output to VCC -	30	30	30	٧
Voltage from collector output to VCC -	50	50	40	٧
Duration of output short-circuit (see Note 4)	10	10	10	s
Continuous total dissipation	Se	e Dissipation F	Rating Table	
Operating free-air temperature range	-55 to '.'	- 25 to 85	0 to 70	°C
Storage temperature range	-65 to ··	-65 to 150	- 65 to 1 50	°C
Case temperature for 60 seconds: FK Package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D or P package		260	260	°C

DISSIPATION RATING TABLE

PACKAGE	TA ≤ 25°C	DERATING	DERATE	TA = 70°C	TA = 85°C	TA = 125°C
PACKAGE	POWER RATING	FACTOR	ABOVE TA	POWER RATING	POAL: RATING	POWER RATING
D	500 mW	5 8 mW/°C	64 °C	464 mW	пW	_
FK	500 mW	11 0 mW/°C	105°C	500 mW	500 mW	275 mW
J (LM111)	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	8.2 mW/°C	89°C	500 mW	500 mW	=
JG (LM111)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	-
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	-
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between VCC+ and VCC-.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 volts, whichever is less.
 - 4. The output may be shorted to ground or either power supply.



electrical characteristics at specified free-air temperature, VCC± = ±15 V (unless otherwise noted)

	PARAMETER	770	T CONDITIONS!		LN	1111 LM	211		LM311		UNIT
	PANAIVIETEN	TES	T CONDITIONS†		MIN	T·Pi	MAX	MIN	TiP:	MAX	UNIT
Vin	Input offset voltage	See Note 5		25°C		0.7	3		2	7.5	mV
VIO	input onset voitage	286 MOLE 2		Full range			4			10	mv
li a	Input offset current	See Note 5		25 °C		4	10		6	50	nA
10	input offset current	See Note 5		Full range	0 = 2		20			70	nA
L-	lanut bing gurant	V 1 V - 14 V		25°C	1	75	100		100	250	nA
lB	Input bias current	$V_0 = 1 \text{ V to } 14 \text{ V}$		Full range			150				ПА
IIL(S)	Low-level strobe current (see Note 6)	V _(strobe) = 0.3 V	, V _{ID} ≤ -10 mV	25°C		-3			-3		mA
	Common-mode				13	13.8		13	13.8		
VICR	input voltage			Full range	to	to		to	to		٧
	range				-14.5	-14.7		-14.5	~14.7		
AVD	Large-signal differential voltage amplification	V _O = 5 V to 35 V	/, R _L = 1 kΩ	25°C	40	200		40	200		V/m\
		Istrobe = -3 mA		25°C		0.2	10				nA
ЮН	High-level (collector)	V _{ID} = 5 mV,	V _{OH} = 35 V	Full range			0.5				μА
	output current	$V_{ID} = 5 \text{ mV},$	V _{OH} = 35 V						0.2	50	nA
			V _{ID} = -5 mV	25°C		0.75	1.5				
	Low-level (collector-	IOL = 50 mA	$V_{ID} = -10 \text{ mV}$	25°C					0.75	1.5	
VOL	to-emitter) output voltage	$V_{CC+} = 4.5 \text{ V},$ $V_{CC-} = 0,$	$V_{ID} = -6 \text{ mV}$	Full range		0.23	0.4				٧
	outhor soliage	IOL = 8 mA	$V_{ID} = -10 \text{ mV}$	Full range					0.23	0.4	
lcc+	Supply current from VCC+, output low	$V_{1D} = -10 \text{ mV},$	No load	25°C		5.1	6		5.1	7.5	mA
lcc-	Supply current from VCC-, output high	V _{ID} = 10 mV,	No load	25°C		-4.1	-5		-4.1	-5	mA

[†]Unless otherwise noted, all characteristics are measured with the balance and balance/strobe terminals open and the emitter output grounded. Full range for LM111 is -55°C to 125°C, for LM211 is -25°C to 85°C, and for LM311 is 0°C to 70°C.

[‡]All typical values are at T_A = 25 °C.

6. The strobe should not be shorted to ground; it should be current driven at -3 to -5 mA, e.g., see Figures 13 and 27.

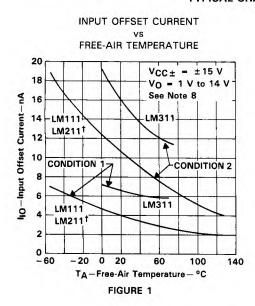
switching characteristics, $V_{CC+} = 15 \text{ V}$, $V_{CC-} = -15 \text{ V}$, $T_A = 25 ^{\circ}C$

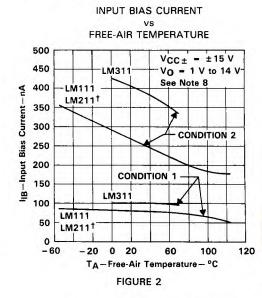
PARAMETER	TEST CONDITIONS	MIN	TYP I	MAX	UNIT
Response time, low-to-high-level output	B 5000 - FV 0 F F 0 - N		115		ns
Response time, high-to-low-level output	$R_C = 500 \Omega$ to 5 V, $C_L = 5 pF$, See Note	'	165		ns

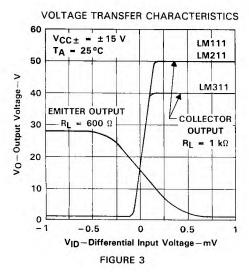
NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

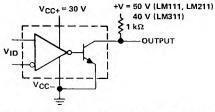


NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pull-up resistor of 7.5 kΩ to V_{CC+}. Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

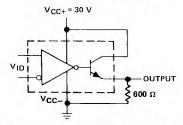








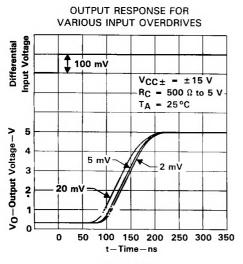
COLLECTOR OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC TEST CIRCUIT FOR FIGURE 3

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. NOTE 8: Condition 1 is with the balance and balance/strobe terminals open. Condition 2 is with the balance and balance/strobe terminals connected to V_{CC+}.

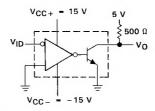




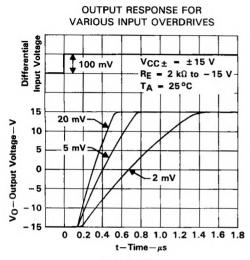
OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES nput Voltage Differential 100 mV VCC± = ±15 V R_C = 500 Ω to 5 V T_A = 25°C Vo-Output Voltage-V 5 4 20mV 3 5 mV - 2 mV 100 150 200 250 300 350 t-Time-ns

FIGURE 4

FIGURE 5



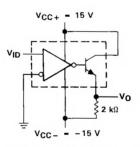
TEST CIRCUIT FOR FIGURES 4 AND 5



VARIOUS INPUT OVERDRIVES input Voltage Differential 100 mV VCC± = ±15 V RF = 2 kΩ to -15 V TA - 25°C 15 2 mV V_O-Output Voltage-V 10 5 mV 5 0 -5 20 mV - 10

OUTPUT RESPONSE FOR

FIGURE 6



-15

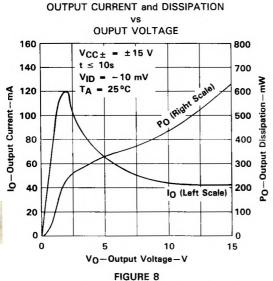
FIGURE 7

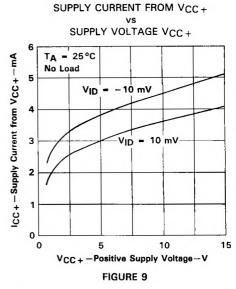
0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8

 $t-Time-\mu s$

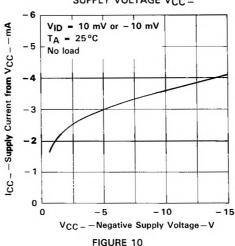








SUPPLY CURRENT FROM V_{CC} – vs SUPPLY VOLTAGE V_{CC} –



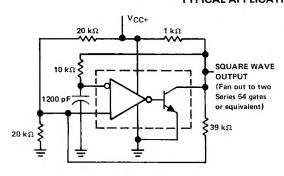


FIGURE 11. 100 kHz FREE-RUNNING MULTIVIBRATOR

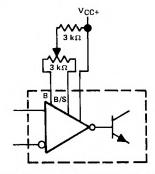


FIGURE 12. OFFSET BALANCING

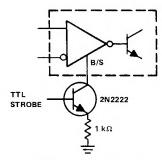


FIGURE 13. STROBING

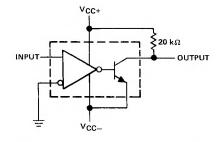
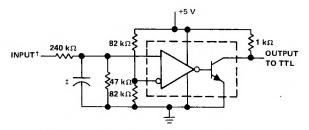


FIGURE 14. ZERO-CROSSING DETECTOR



[†]Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.

FIGURE 15. TTL INTERFACE WITH HIGH-LEVEL LOGIC



[‡]May be added to control speed and reduce susceptibility to noise spikes.

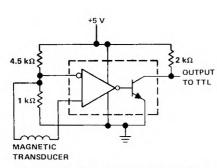


FIGURE 16. DETECTOR FOR MAGNETIC **TRANSDUCER**

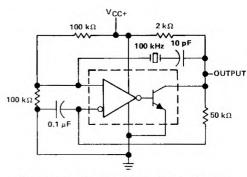
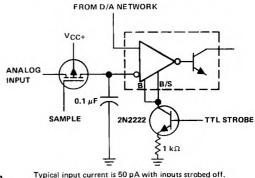


FIGURE 17. 100 kHz CRYSTAL OSCILLATOR

1N4001 -OUTPUT TIP30 INPUT

FIGURE 18. COMPARATOR AND SOLENOID DRIVER



Typical input current is 50 pA with inputs strobed off. FIGURE 19. STROBING BOTH INPUT AND **OUTPUT STAGES SIMULTANEOUSLY**

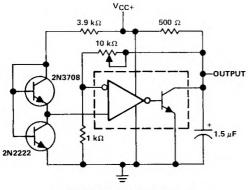


FIGURE 20. LOW-VOLTAGE ADJUSTABLE REFERENCE SUPPLY

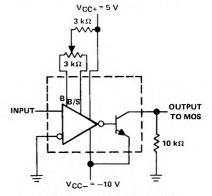
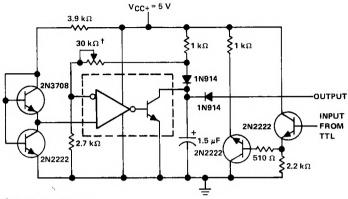


FIGURE 21. ZERO-CROSSING DETECTOR DRIVING MOS LOGIC





[†]Adjust to set clamp level.

FIGURE 22. PRECISION SQUARER

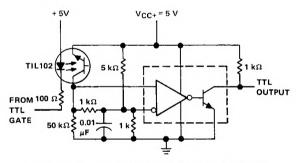


FIGURE 23. DIGITAL TRANSMISSION ISOLATOR

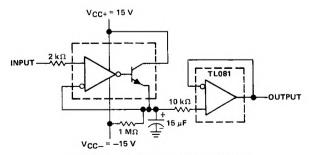


FIGURE 24. POSITIVE-PEAK DETECTOR



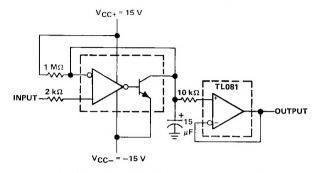
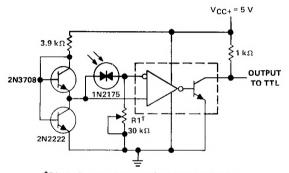
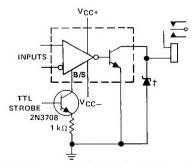


FIGURE 25. NEGATIVE-PEAK DETECTOR



[†]R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it decreasing dark current by an order of magnitude.

FIGURE 26. PRECISION PHOTODIODE COMPARATOR



‡Transient voltage and inductive kickback protection

FIGURE 27. RELAY DRIVER WITH STROBE



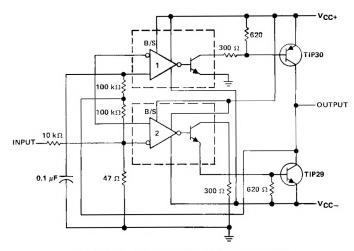


FIGURE 28. SWITCHING POWER AMPLIFIER

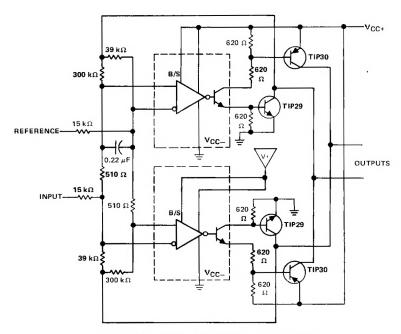


FIGURE 29. SWITCHING POWER AMPLIFIERS



LM139, LM239, LM339, LM139A LM239A, LM339A, LM2901 QUADRUPLE DIFFERENTIAL COMPARATORS

D1979, OCTOBER 1979-REVISED APRIL 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- . Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM139)
- . Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage

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Output Compatible with TTL, MOS, and CMOS

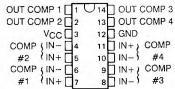
These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 3 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

			PACE	KAGE	
TA	V _{IO} MAX at 25°C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to	5 mV	LM339D	<u>-</u>	LM339J	LM339N
70°C	2 mV	LM339AD	-	LM339AJ	LM339AN
−25°C to	5 mV	LM239D	-	LM239J	LM239N
85°C	2 mV	LM239AD	-	LM239AJ	LM239AN
-40°C to 125°C	7 mV	LM2901ID	=	LM2901IJ	LM2091 IN
−55°C to	5 mV	-	LM139FK	LM139J	-
125°C	2 mV		LM139AFK	LM139AJ	-

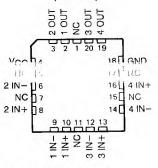
The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM339DR) $\,$

LM139, LM139A . . . J PACKAGE ALL OTHERS . . . D, J, OR N PACKAGE (TOP VIEW)



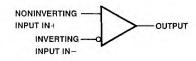
LM139, LM139A FK CHIP CARRIER PACKAGE

(TOP VIEW)



NC-No internal connection

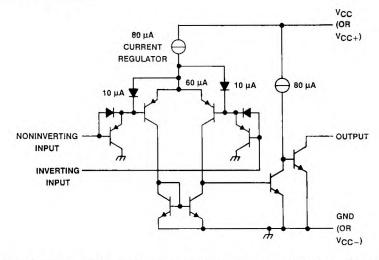
symbol (each comparator)



PROPUL-10K DATA documents contain information in the state of publication date. Products conform to product the propulation publication processing does not necessarily include testing of all parameters.



schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 2)
Differential input voltage (see Note 3)
Input voltage range (either input)
Output voltage
Output current
Duration of output short-circuit to ground (see Note 4) unlimited
Continuous total dissipation
Operating free-air temperature range: LM139
LM239, LM239A
LM339, LM339A 0°C to 70°C
LM290140°C to 125°C
Storage temperature range
Case temperature for 60 seconds: FK package
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package

NOTES: 2. All voltage values, except differential voltages, are with respect to the network ground terminal.

- 3. Differential voltages are at the noninverting input terminal with respect to the inverting input.
- 4. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWER RATING	T _A = 125°C POWER RATING
D	900 mW	7.6 mW/°C	31°C	608 mW	494 mW	
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM139, LM139A)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (All others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	_
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	



LIND E,

		+	7	LM139		_	LM139A		1000
PAHAMEIEH	IESI CONDITIONS		MIN	ТУР	MAX	MIN TYP MAX MIN TYP MAX	TYP	MAX	5
	$V_{CC} = 5 \text{ V to } 30 \text{ V,}$	25°C		2	5		-	2	New
VIO Input offset voltage	$V_{IC} = V_{ICR} min$, $V_{O} = 1.4 V$	-55°C to 125°C			6			4	2
		25°C		က	22		က	25	
IO Input offset current	VO = 1.4 V	-55°C to 125°C			100			100	<u> </u>
		Cano		r	2007			uc	90

			+ 0	LM139	•	5	LM139A		-
	PARAMETER	TEST CONDITIONS	2	MIN TYP	WAX C	Z	TYP	MAX	
1		$V_{CC} = 5 \text{ V to 30 V,}$	25°C		2 5		-	2	Var
	VIO Input offset voltage	VIC = VICR min, VO = 1.4 V	-55°C to 125°C		0			4	2
1			25°C		3 25		က	25	4
	Input offset current	VO = 1.4 V	-55°C to 125°C		100			100	<u> </u>
1			25°C	-25	5 -100		-25	-100	<
	Input bias current	VO = 1.4 V	-55°C to 125°C		-300			-300	2
1			Canc	0 to		0 to			
			28	VCC-15		VCC-1.5			^
	VICR Common-mode input voltage range		Cand F - 1 Conn	0 to		0 to			>
			255.0101255-	VCC-2		VCC-2			
1	Large-signal differential voltage	$V_{CC\pm} = \pm 7.5 \text{ V},$ $V_{CC\pm} = \pm 7.5 \text{ V},$	25°C	200	0	90	200		V/m/V
- 1	andmicanon	\$ C 2 C - O	2000						4
	High found contents are	V= +1V	25°C	0.1	100		0.1		Y
	Digitalevel output content	$V_{OH} = 10$	-55°C to 125°C		-			-	нΑ
1			25°C	150	0 400		150	400	Van
	VOL Low-level output voitage	VID = -1 V, (OL = 4 IIIA	-55°C to 125°C		700			700	•
1	Low-level output current	$V_{1D} = -1 V$, $V_{OL} = 1.5 V$	25°C	6 1	16	9	16		μM
	Supply current	$V_Q = 2.5 \text{ V}$, No load	25°C	8.0	8 2		0.8	2	mA

All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, VCC = 5 V, TA = 25°C

LAUANELLE		TEST CONDITIONS	MIN	TYP MAX	MAX
	R _L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3	
Hesponse inne	C _L = 15 pF, [‡] See Note 4	TTL-tevel input step		0.3	

‡ CL includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

Voltage Comparators

electrical characteristics at specified free-air temperature, VCC = 5 V (unless otherwise noted)

	The same of the sa	-	TOMOTHUM TOTAL		LM2	LM239, LM339	6	LM23	LM239A, LM339A	19A		LM2901		FILM
	PARAMEICH	<u> </u>	i conditions	Y	MIN	TYP	MAX	MIN	ΥF	MAX	MIN	ΗV	MAX	5
	Input offset	VCC = 5 V to 30 V,	۷,	25°C		2	5		-	2		2	7	1
0	voltage	VIC = VICR min,	$V_0 = 1.4 \text{ V}$	Full range			6			4			15)E
	Input offset	7, 7,		25°C		2	20		D.	22		2	20	
0	current	VO = 1.4 V		Full range			150			150			200	Ę
	The state of the s			25°C		-25	-250		-25	-250		-25	-250	<
<u>B</u>	niput plas current	Vo = 1.4 V		Full range			-400			-400			-500	=
				25°C	0 to			0 to			0 to			
Mon					VCC-1.5			VCC-15			Vcc-1.5			1
3				First contract	0 to			0 to			0 to			
	range			ruii iaiige	VCC-2			VCC-2			VCC-2			
	Large-signal	VCC = 15 V,												
AVD	differential voltage $V_Q = 1.4 \text{ V to } 11.4 \text{ V},$	Vo = 1.4 V to 11.	.4 V,	25°C	20	200		20	200		25	100		V/mV
	amplification	RL = 15 KD to VCC	8											
	High-level	Vin - 1 V	VOH = 5 V	25°C		0.1	20		0.1	22		0.1	20	υĄ
5	output current	·	$V_{OH} = 30 V$	Full range			-			-			-	нА
	Low-level	14.	1	25°C		150	400		150	400		150	200	1
ý	output voltage	'\D = - \'.	10L = 4 IIIA	Full range			700			200			200	È
길	Low-level output current	$V_{\text{ID}} = -1 \text{ V},$	V _{OL} = 1.5 V	25°C	9	16		9	91		9	16		Ψ
١,	Supply current	Vo = 2.5 V, No load	pad	Couc		9.0	2		0.8	2		0.8	2	{
2	(four comparators) $V_{CC} = 30 \text{ V}$, $V_{O} = 15 \text{ V}$, No load	VCC = 30 V, VO	= 15 V, No load	2 2 2								-	2.5	=

zero common-mode input voltage unless otherwise specified.

25°C 11 5 V, TA II switching characteristics, VCC

PAHAMETER		TEST CONDITIONS	Z	MIN TYP MAX	MAX
only constructed	RL connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive		1.3	
anin asnodsau	C ₁ = 15 pF, [‡] See Note 5	TTL-level input step		0.3	

UNIT his

⁺ CL includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

LM193, LM293, LM393, LM293A, LM393A, LM2903 DUAL DIFFERENTIAL COMPARATORS

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Tvp
- Low Input Offset Current . . . 3 nA Typ (LM139)
- Low Input Offset Voltage . . . 2 mV Tvp
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

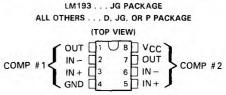
description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 8 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

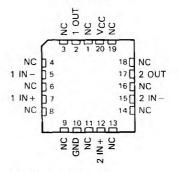
SYMBO	LIZATION	OPERATING	VIO MAX
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE	AT TA = 25°C
LM193	L, FK, JG	-55°C to 125°C	5 mV
LM293	D, JG, P	-25°C to 85°C	5 mV
LM293A	D, JG, P	-25°C to 85°C	2 mV
LM393	D, JG, P	0°C to 70°C	5 mV
LM393A	D, JG, P	0°C to 70°C	2 mV
LM2903	D, JG, P	-40°C to 125°C	7 mV

The D package is available in tape and reel. Add an R suffix when ordering. (e.g., LM393DR)



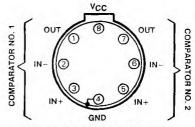
D2232, JUNE 1976-REVISED NOV "

LM193 . . . FK PACKAGE (TOP VIEW)



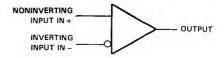
NC-No internal connection

LM193 . . . L PLUG-IN PACKAGE (TOP VIEW)

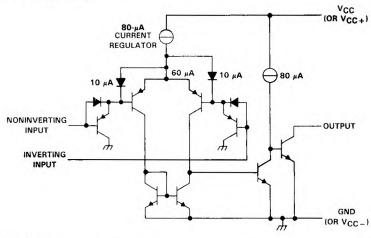


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

symbol (each comparator)



schematic (each comparator)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supp	oly voltage, V _{CC} (see Note 1)
Differ	rential input voltage (see Note 2)
Input	voltage range (either input)
Outp	ut voltage
	ut current
Dura	tion of output short-circuit to ground (see Note 3)
	inuous total dissipation
Oper	rating free-air temperature range: LM193
	LM293, LM293A ~25°C to 85°C
	LM393, LM393A 0°C to 70°C
	LM290340°C to 125°C
Stora	age temperature range65°C to 150°C
Case	temperature for 60 seconds: FK package
Lead	temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260°C
Lead	temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package
Lead	temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
 - 3. Short circuits from outputs to VCC can cause excessive heating and eventual destruction.

DISSIPATION RAYING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	TA = 125°C POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW	377 mW	_
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
JG (LM193)	900 mW	8.4 mW/°C	43°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	-
L	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
P	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	-



LIND ris m

LM2903 LM293, LM393 LM393A, LM393A electrical characteristics at specified free-air temperature, VCC = 5 V (unless otherwise noted)

	DADAMETER	TECT COMPLETIONS	Nic+				1					-	-	1000		2
	LANAMETEN			Z	TYP MAX		MIN	TYP MAX	MAX	NIM	TYP MAX	MAX	NIM	TYP MAX	Ž	;
1		VCC = 5 V to 30 V,	25°C		2	2		2	2		-	2		2	7	2
	input onset voitage	VIC = VICH. VO = 1.4 V	Full range			6			o			4			15	
1	2		25°C		3	83		ທ	20		ഗ	20		S	20	<
	input offset current	VO = 1.4 V	Full range			100			150			150			200	<u> </u>
1	A	74.	25°C		25	100		52	250		52	250		52	520	90
	input bias current	V + .: = OV	Full range			300			400			400			200	
			25°C	0 to												
	Common-mode input voltage			Vcc-1.5		×	VCC-1.5			VCC-1.5		^	VCC-1.5			>
VICR.	range‡			0 to			0 to			0 to			0 to		1	
			rull range	VCC-2		_	VCC-2			VCC-2			VCC-2			
	large stone differential	V _{CC} = 15 V,														
	voltage amplification	V _O = 1.4 V to 11.4 V,	. 25°C	20	200	-	20	200		20	200		52	100	-	V/m/V
1		VOH = 5 V VID = 1 V	25°C		0.1			0.1	20		0.1	20		0.1	99	An
	High-level output current		Full range			-			٠			-			-	¥
1		7. 4 - 4	25°C		150	400		150	400		150	400		150	400	74
	Low-level output voltage	lOL = 4 mA, VID = -1 V,	Full range			200			700			200			200	1
1	Low-level output current	$V_{OL} = 1.5 \text{ V}, V_{ID} = -1 \text{ V}$	25°C	9			9			9			9			mA
1		VCC = 5 V	25°C		9.0	F		0.8	-	2000	0.8	1		8 0	-	V W
	Supply current	NCC = 30 V Full range	Full range			25			2.5			2.5			2.5	<u> </u>

characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} + -1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, VCC = 5 V, TA = 25°C

ARAMETER		TEST CONDITIONS	Z	TYP	YP MAX
	RL connected to 5 V through 5.1 kD,	100-mV input step with 5-mV overdrive		1.3	
esponse time	C ₁ = 15 pF, [§] See Note 4	TTL-level input step		0.3	

9 CL includes probe and jig capacitance.
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

LM3302 QUADRUPLE DIFFERENTIAL COMPARATOR

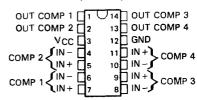
D2402, OCTOBER 1977 - REVISED APRIL 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 28 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ
- Low Input Offset Voltage . . . 3 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±28 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

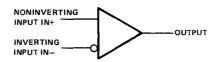
description

This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 28 V and pin 3 is at least

D, J, OR N PACKAGE (TOP VIEW)



symbol (each comparator)

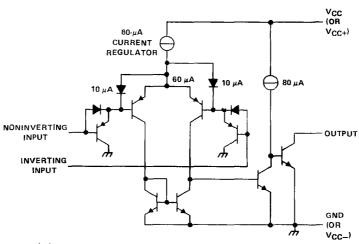


AVAILABLE OPTIONS

SYMBO	LIZATION	OPERATING	
DEVICE	PACKAGE SUFFIX	TEMPERATURE RANGE	V _{IO} MAX at 25°C
LM3302	D, J, N	-40°C to 85°C	20 mV

The D packages are available taped and reeled. Add the suffix R to the device type, when ordering. (i.e., LM3302DR)

1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.



Current values shown are nominal.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)
Differential input voltage (see Note 2) ±28 V
Input voltage range (either input)
Output voltage
Output current
Duration of output short-circuit to ground (see Note 3) unlimited
Continuous total dissipation
Operating free-air temperature range40°C to 85°C
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.

- 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
- 3. Short circuits from the output to VCC can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics at specified free-air temperature, VCC = 5 V (unless otherwise noted)

	PARAMETER	1	EST CONDITION	ıst	MIN	TYP	MAX	UNIT
.,	land offers with a	V _{CC} = 5 V to		25°C		3	20	.,
VIO	Input offset voltage	$V_{IC} = V_{ICR} m$ $V_{O} = 1.4 V$	in,	-40°C to 85°C			40	mV
10	Input offset current	V _O = 1.4 V		25°C		3	100	nA
10	input onset current	VO = 1.4 V		-40°C to 85°C			300	1110
lв	Input bias current			25°C		-25	500	пA
'IB	input bias current			-40°C to 85°C			-1000	HA.
				25°C	0 to			
VICR	Common-mode input			230	V _{CC} -1.5			v
VICH	voltage range			-40°C to 85°C	0 to			
		1		-40 C to 65 C	Vcc-2			
AvD	Large-signal differential voltage amplification	$V_{CC} = 15 \text{ V},$ $V_{O} = 1.4 \text{ V to}$ $R_{L} = 15 \text{ k}\Omega \text{ to}$		25°C	2	30		V/mV
				25°C		0.1		nA
ЮН	High-level output current	$V_{ID} = 1 V$	V _{OH} = 5 V	-40°C to 85°C			1	μА
V	Low-level output voltage	V 1 V	l _{OL} = 4 mA	25°C		150	500	mV
VOL	Low-level output voltage	$V_{ID} = 1 V$	IOL = 4 IIIA	40°C to 85°C			700	mv
lol	Low-level output current	V _{ID} = 1 V,	V _{OL} = 1.5 V	25°C	6	16		mA
loc	Supply current	VO = 25 V.	No load	25°C		0.8	2	mA
1CC	(four comparators)	VO = 25 V,	INO IOAU	23 0		0.6	2	""

[†] All characteristics are measured with zero common-mode input voltage unless otherwise specified.



LM3302 QUADRUPLE DIFFERENTIAL COMPARATOR

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	ONDITIONS	MIN	TYP	MAX	UNIT
Decrease time	$R_L = 5.1 \text{ k}\Omega \text{ to 5 V},$		100-mV input step with 5-mV overdrive		1.3		
Response time	$C_L = 15 pF^{\ddagger}$,	See Note 4	TTL-level input step		0.3		μs

‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



LP111, LP211, LP311 LOW-POWER DIFFERENTIAL COMPARATORS WITH STROBES

D3019, JUNE 1987-REVISED MAY 1988

- Low Power Drain 900 μW Typical with 5-V Supply
- Operates from ±15 V or from a Single Supply as Low as 3 V
- Output Drive Capability of 25 mA
- Emitter Output Can Swing Below Negative Supply
- Response Time 1.2 μs Typ
- Low Input Currents:

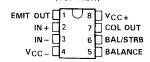
Offset Current . . . 2 nA Typ Blas Current . . . 15 nA Typ

- Wide Common-Mode Input Range:
 14.5 V to 13.5 V with ± 15-V Supply
- Same Pinout as LM111, LM211, LM311
- Designed to be Interchangeable with National Semiconductor LP311

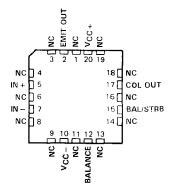
description

The LP111, LP211, and LP311 are a low-power versions of the industry-standard LM111, LM211, and LM311. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption but only a 6:1 slowdown in response time. Thus, they are well-suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from $\pm 18 \ V$ down to a single 3-V supply with less than 300 μA current drain, but are still capable

LP111 . . . JG DUAL-IN-LINE PACKAGE LP211, LP311 . . . D, JG, OR P PACKAGE (TOP VIEW)

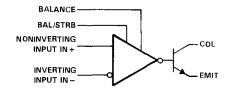


LP111 . FK CHIP CARRIER PACKAGE (TOP VIEW)



NC-No internal connection

functional block diagram



AVAILABLE OPTIONS

	V - MAY	PACKAGE							
TA	VIO MAX AT 25°C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)				
0°C to 70°C	7 5 mV	LP311D		LP311JG	LP311P				
- 25°C to 85°C	7.5 m V	LP211D	-	LP211JG	LP211P				
- 55 °C to 125 °C	7 5 mV	_	LP111FK	LP111JG					

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., LP311DR)



description (continued)

of driving a 25-mA load. The LP111, LP211, and LP311 are quite easy to apply free of oscillation if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins.

The LP111 is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The LP211 is characterized for operation from $-25\,^{\circ}$ C to 85 °C, and the LP311 is characterized for operation from 0 °C to 70 °C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC+ (see Note 1) .		18 V
	1 and 3)	
Voltage from collector output to VCC		40 V
Voltage from collector output to emitt	ter output	40 V
Duration of output short-circuit (see N	lote 4)	40 V
Continuous total dissipation		ssipation Rating Table
Operating free-air temperature range:	LP111	55°C to 125°C
	LP211	25°C to 85°C
	LP311	0°C to 70°C
Storage temperature range		65°C to 150°C
Lead temperature 1,6 mm (1/16 inch)	from case for 10 seconds: D or P package	e 260°C
Case temperature for 60 seconds: FK	package	260°C
Lead temperature 1,6 mm (1/16 inch)	from case for 60 seconds: JG package .	300°C

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between VCC+ and VCC-.
 - 2. Differential input voltages are at the noninverting input terminal with respect to the inverting terminal.
 - 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
 - 4. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	_
FK	1375 mW	11.0 mW/°C	25 °C	880 mW	715 mW	275 mW
JG (LP111)	1050 mW	8.4 mW/°C	25 °C	672 mW	546 mW	210 mW
JG (LP_11)	825 mW	6.6 mW/°C	25 °C	528 mW	429 mW	-
P	500 mW	8.0 mW/°C	88 °C	500 mW	500 mW	-

recommended operating conditions

	MIN N	IOM MAX	UNITS
Input voltage (V _{CC±} ≤15 V)	V _{CC} _ +0.5	V _{CC+} -1.5	V
Supply voltage, V _{CC+} - V _{CC-}	3.5	30	V



LP111, LP211, LP311 LOW-POWER DIFFERENTIAL COMPARATORS WITH STROBES

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15 \text{ V}$ (unless otherwise noted)

	PARAMETER		TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT
V/		RS < 100 kΩ.	Con Note E	25°C			2	7.5	mV
VID	Input offset voltage	HS < 100 KU,	See Note 5	Full Range				10	mv
	1	Can Nata E		25°C			2	25	
10	Input offset current	See Note 5		Full Range				35	nA
	1			25 °C			15		^
IВ	Input bias current	The second second		Full Range	Full Range			150	nA
	Low-level output voltage	V _{ID} > 10 mV, See Note 6	I _{OL} = 25 mA,	25°C			0.4	1.5	
VOL		$V_{CC} = 4.5 \text{ V},$	$V_{CC-} = 0$,		LP111		0.1	0.7	V
		V _{ID} < -10 mV, See Note 6	$I_{OL} = 1.6 \text{ mA},$	Full Range	LP211 LP311		0.1	0.4	
	Low-level strobe current	V _(strobe) = 0.3 V, See Note 7	$V_{\text{ID}} < -10 \text{ mV},$	25°C			100	300	μА
IO(off)	Output off-state current	$V_{\text{ID}} > 10 \text{ mV},$	V _{CE} = 35 V	25°C			0.2	100	nA
AVD	Large signal differential voltage amplification	R _L = 5 kΩ		25°C		40	100		V/mV
ICC+	Supply current from VCC+	$V_{ID} = -50 \text{ mV},$	R _L = ∞	Full Range			150	300	μΑ
Icc-	Supply current from VCC-	$V_{ID} = 50 \text{ mV},$	R _L = ∞	Full Range			-80	-180	μΑ

 $^{^{\}dagger}$ All typical values are at $V_{CC\pm} = \pm 15 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$.

- NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
 - , 6. Voltages are with respect to EMIT OUT and $V_{\mbox{CC}}$ tied together.
 - 7. The strobe should not be shorted to ground; it should be current driven at 100 μ A to 300 μ A.

switching characteristics at V_{CC±} = ±15 V, T_A = 25 °C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP MA	X UNIT
Response time	See Note 8		1.2	μS

NOTE 8: The response time is specified for a 100-mV input step with 5-mV overdrive.

LP239, LP339, LP2901 LOW-POWER QUAD DIFFERENTIAL COMPARATORS

D3044, OCTOBER 1987-REVISED MAY 1988

•	Ultralow Power Supply Current Drain Typically 60 µA	D, J, OR N PACKAGE (TOP VIEW)
•	Low Input Biasing Current 3 nA	OUT COMP 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
•	Low Input Offset Current ± 0.5 nA	VCC 3 12 GND
•	Low Input Offset Voltage ±2 mV	COMP #2 $\begin{cases} IN - 4 & 11 IN + \\ IN + 5 & 10 IN - \end{cases}$ COMP #4
•	Common-Mode Input Voltage Includes Ground	COMP #1 $\begin{cases} IN - \begin{vmatrix} 1 & 9 \\ IN + \end{vmatrix} & 9 \begin{vmatrix} IN + \\ IN + \end{vmatrix} & COMP #3 \end{cases}$

- Output Voltage Compatible with MOS and CMOS Logic
- High Output Sink-Current Capability
 (30 mA at V_O = 2 V)
- Power Supply Input Reverse-Voltage Protected
- Single-Power-Supply Operation
- Pin-for-Pin Compatible with LM239, LM339, LM2901

description

The LP239, LP339, and LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw $60-\mu$ A drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultralow power supply drain current is independent of the power supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time delay generators, voltage controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, and LP2901 were specifically designed to interface with the CMOS logic family. The ultralow power supply current makes these products desirable in battery-powered applications.

The LP239 is characterized for operation from -25 °C to 85 °C. The LP339 is characterized for operation from 0 °C to 70 °C. The LP2901 is characterized for operation from -40 °C to 85 °C.

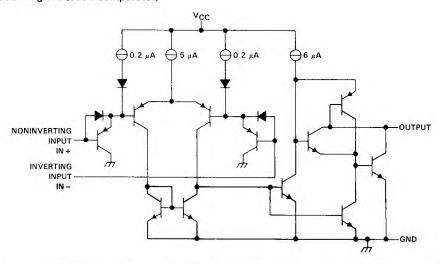
AVAILABLE OPTIONS

	VIO MAX AT 25°C S																		
TA		SMALL-OUTLINE (D)	PLASTIC DIP	CERAMIC DIP (J)															
0°C to 70°C	±5 mV	LP339D	LP339N	LP339J															
- 25°C to 85°C	±5 mV	LP239D LP239N	LP239D LP239N	LP239D LP239N		LP239D LP239N		LP239D LP239N		LP239D LP239N		LP239D LP239N		LP239D LP239N		LP239D LP239N		LP239J	
-40°C to 85°C	±5 mV	LP2901D	LP2901N	LP2901J															

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., LP339DR).



schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Differential input voltage, VID (see Note 2)
Input voltage range (either input)
Input current, V _I ≤ -0.3 V (see Note 3)
Duration of output short-circuit to ground (see Note 4) unlimited
Continuous total dissipation (see Note 5) See Dissipation Rating Table
Operating free-air temperature range: LP23925 °C to 85 °C
LP339
LP2901
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.

2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

- 3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive and normal output states are re-established when the input voltage returns to a value more positive than -0.3 V at T_A = 25°C.
- 4. Short circuits between outputs to VCC can cause excessive heating and eventual destruction.
- If the output transistors are allowed to saturate, the low bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8 2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW



LP239, LP339, LP2901 LOW-POWER QUAD DIFFERENTIAL COMPARATORS

recommended operating conditions

			LP2901		7 6 -	LP239		LP339			HAUT
		MIN	NOM	MAX	w.	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		5		30			30	5		30	٧
	Vcc = 5 V	0		3	0		3	0		3	٧
Common-mode input voltage, VIC	V _{CC} = 30 V	0		28	0		28	.0		28	٧
	V _{CC} = 5 V	0		3	0		3	0		3	٧
Input voltage, V _I	V _{CC} = 30 V	0		28	0		28	0		28 3 28	٧
Operating free-air temperature, TA		-40		85	-25		85	0		70	°C

electrical characteristics, VCC = 5 V, TA = 25 °C (unless otherwise noted)

	PARAMETER	TES	ST CONDITION	S	MIN	TYP	MAX	UNIT
·/·-	1	$V_{CC} = 5 \text{ V to } 30 \text{ V}, V_{O} = 2$		25°C		±2	±5	mV
VIO	Input offset voltage	RS = 0,	See Note 6	Full range			±9	7 mv
				25°C		±0.5	±5	
IO	Input offset current			Full range		±1	±15	nA
	1. 2. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	Con Mario 7		25°C		-2.5	- 25	
IB	Input bias current	See Note 7	Full range		-4	-40	nA	
	Common-mode input			25°C	0 to V _{CC} - 1.5			V
VICR	voltage range	Single supply		Full range	0 to V _{CC} - 2			7 "
AVD	Large-signal differential voltage amplification	$V_{CC} = 15 \text{ V}, \qquad R_L = 15 \text{ k}\Omega$				500		V/mV
		V ₁₋ = 1 V,	V _O = 2 V	25°C	20	30		
	Output sink current		(see Note 8)	Full a	15			mA
		$V_{I+} = 0$	$V_0 = 0.4 \text{ V}$	2	0.2	0.7		
	O the state of the	$V_{I+} = 1 V$	V ₀ = 5 V	25°C		0.1		nA
	Output leakage current	$V_{I-} = 0$	V _O = 30 V	Full range			1	μΑ
VID	Differential input voltage	V _I ≤ 0 (or V _{CC} – on	V _I ≤ 0 (or V _{CC} – on split supplies)				36	V
Icc	Supply current	R _L = ∞ all comparate	ors			60	100	μΑ

NOTES: 6. ViO is measured over the full common-mode input voltage range.

- 7. Because of the p-n-p input stage, the direction of the current is out of the device. This current is essentially constant (i.e., independent of the output state). Therefore, no loading change exists on the reference or input lines as long as the commonmode input voltage range is not exceeded.
- The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them
 to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V, and smaller currents at output voltages
 less than 1.5 V.

switching characteristics, VCC = 5 V, TA = 25 °C, RL connected to 5 V through 5.1 k Ω

PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
Large-signal response time	TTL logic swing, V _{ref} = 1.4 V	1.3	μS
Response time		8	μS



FIGURE 1. BASIC COMPARATOR

FIGURE 2. CMOS DRIVER

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V. It is usually necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than -0.3 V. The output section has two distinct modes of operation: a Darlington mode and a grounded-emitter mode. This unique drive circuit permits the device to sink 30 mA at $V_{Q}=2$ V in the Darlington mode and 700 μ A at $V_{Q}=0.4$ V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the hFE of Q1, the hFE of Q2, and I1 and by the 60- Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc., in this mode while maintaining an ultralow power supply current of 60 μ A typically.

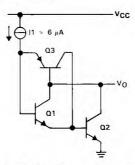


FIGURE 3. OUTPUT SECTION SCHEMATIC DIAGRAM

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the hep of Q2 (700 μ A at V0 = 0.4 V). The output of the devices exhibit a bimodal characteristic with a smooth transition between modes.

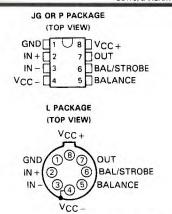
In both cases, the output is an uncommitted collector. Therefore several outputs can be tied together to provide a dot logic function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range, and there is no restriction on this voltage based on the magnitude of the voltage that is applied to the VCC terminal of the package.



- Low Input Offset Voltage . . . 1.5 or 0.5 mV Max
- . Maximum Input Bias Current . . . 50 or 25 nA
- . Low Input Offset Current . . . 4 or 3 nA Max
- Output Response Time . . . 250 ns Max
- Voltage Gain . . . 200 V/mV Min
- . . . 50 mA Source or Sink
- Differential Input Voltage . . . ±30 V
- Can Operate from Single 5-V Supply
- Pin-Compatible with LM111 Series
- Designed to be Interchangeable with Linear Technology LT1011 and LT1011A

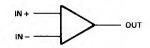
description

The LT1011 and LT1011A are general-purpose comparators that are pin-compatible with the LM111. The LT1011A offers significantly better input characteristics than the LM111: four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Additionally, the supply current is considerably lower than that of the LM111 with no loss in speed. The offset voltage temperature coefficient of the LT1011A is 15 $\mu\text{V/}^{\circ}\text{C}$. The LT1011 and LT1011A are fully specified for dc parameters and output response time when operating from a single 5-V supply.



Pin 4 (L package) is in electrical contact with the case.

symbol



The LT1011 and LT1011A can be used in high-accuracy (\geq 12-bit) systems without trimming. The devices retain all the versatile features of the LM111 including single-supply operation (3 V to 36 V) or dual-supply operation (\pm 1.5 V to \pm 18 V) and a floating transistor output with 50-mA source or sink capability. The devices can drive loads that are referenced to ground, the negative supply, or the positive supply, and are specified up to 50 V between VCC— and the collector output. A differential input voltage up to the full supply voltage is allowed, even with \pm 18-V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C. C-suffix devices are characterized for operation from 0°C to 70°C.

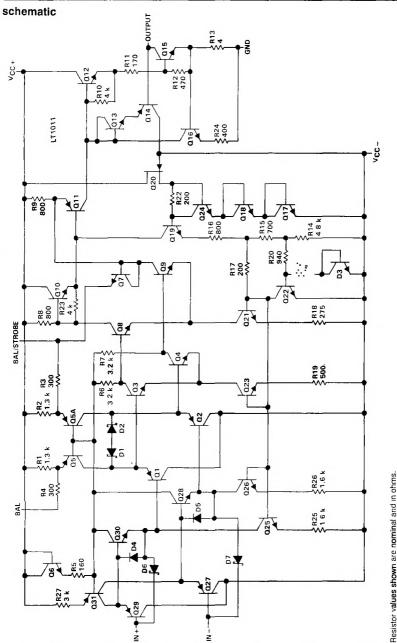
AVAILABLE OPTIONS

		PACKAGE						
TA	V _{IO} MAX at 25°C	CERAMIC DIP (JG)	METAL CAN	PLASTIC DIP				
0°C τc 70°C	1.5 mV 0.5 mv	LT1011CJG LT1011ACJG	LT1011CL LT1011ACL	LT1011CP LT1011ACP				
-55°C to 125°C	1.5 mV 0.5 mV	LT1011MJG LT1011AMJG	LT1011ML LT1011AML					

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Supply voltage, VCC+ 18 V Supply voltage, VCC- -18 V
Voltage from output to VCC—: M-suffix
C-suffix
Voltage from GND to VCC
Voltage from strobe to VCC+ 5 V
Differential input voltage (see Note 1) ±36 V
Input voltage (either input, see Note 2)
Duration of output short circuit (see Note 3)
Continuous power dissipation See Dissipation Rating Table
Operating free-air temperature range: M-suffix
C-suffix
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 2. Inputs may be clamped to supplies with diodes so that the maximum input voltage actually exceeds the supply voltage by one diode drop (refer to "input protection" in the applications section).
 - 3. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR	T _A = 70°C	TA = 125°C
PACKAGE	POWER RATING	ABOVE TA = 25°C	POWER RATING	POWER RATING
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	N/A
Р	1000 mW	8.0 mW/°C	640 mW	N/A

recommended operating conditions

		N	M-SUFFIX			C-SUFFIX			
		MIN	NoM	MAX	MIN	NOM	MAX	UNIT	
Supply voltage, V _{CC+}				15			15	٧	
Supply voltage, VCC				-15			-15	V	
	V _{CC±} = ±15 V	14.5		13	-14.5		13	3 ,,	
Input voltage, V _I , (see Note 4)	V _{CC} = single 5-V	0.5		3	0.5		3	V	
Operating free-air temperature, TA	· · · · · · · · · · · · · · · · · · ·	55		125	0		70	°C	

NOTE 4: See "Input Signal Range" under "Typical Application Data."

electrical characteristics, $V_{CC\pm}=\pm15$ V, $V_{IC}=0$, Rs = 0, pin 1 at V_{CC-} , output at pin 7 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TAT	2	.T1011		L	T1011/	4	UNI	
	PARAMETER	TEST CONDITIONS	'A'	MIN	TYP	MAX	MIN	TYP	MAX	UNI	
		I- 45-4 V 0	25°C		0.6	1.5		0.3	0.5	. 33	
	form a Management	$I_{O} = 1.5 \text{ mA}, V_{O} = 0$	Full range			3			1		
Vio	Input offset voltage	D = 5010 0 - Note 5	25°C			2			0.75	mV	
		$R_S \le 50 \text{ k}\Omega$, See Note 5	Full range			3			1.5		
αVIO	Average temperature coefficient of input offset voltage	See Note 6	Full range		4	25		4	15	μV/°(
lia.	Input offset current	See Note 5	25°C		0.2	4		0.2	3	пA	
NO	input onset current	269 140/6 2	Full range			6	200		5	IIA	
		IO = 1.5 mA, VO = 0	25°C		-20	±50		-15	±25		
liB	Input bias current	See Note 5	25°C		-25	±65		-20	±35	nA	
		See Note 5	Full range			±80			±50		
IL(S)	Low-level strobe current (See Note 7)		25°C			-500			-500	μА	
VICR	Common-mode input voltage range		Full range	-14.5 to 13			-14.5 to			V	
AVD	Large-signal differential voltage amplification	$R_L = 1 k\Omega \text{ to V}_{CC+}$, $V_O = -10 \text{ V to 14.5 V}$	25°C	200	500		200	500		V/m	
VOL	Low-level output voltage	$V_{ID} = -5 \text{ mV}, I_{OL} = 8 \text{ mA},$ Pin 1 at 0 V	Full range			0.4			0.4	V	
VOL	Low-level output voltage	$V_{ID} = -5 \text{ mV}$, $I_{OL} = 50 \text{ mA}$, Pin 1 at 0 V	Full range			1.5			1.5		
low.	Output leakage current	V _{ID} = 5 mV, Pin 1 at -15 V,	25°C		0.2	10		0.2	10	nA	
O(lkg)	Curput loanage Current	$V_0 = 35 \text{ V } (25 \text{ V for LT1011C})$	Full range			500			500	1100	
CMRR	Common-mode rejection ratio	VIC = VICR min, RS ≤ 50 kΩ	25°C	90	115		94	115		dB	
CC+	Supply current from VCC+		25°C		3.2	4		3.2	4	mA	
lcc-	. /c from VCC-		25°C		-1.7	-2.5		-1.7	-2.5	m/	
Ci	Input capacitatice		25°C		6	- 11		6		pF	

[†] Full range is -55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

- NOTES: 5. These specifications apply for single supply voltages from 5 V to 30 V and dual supply voltages from ±2.5 V to ±15 V for the entire input voltage range, and for both high and low output states. The high state is I_{OH} ≥ 100 µA and V_O ≥ (V_{CC+} − 1 V). The low state is I_{OL} ≤ 8 mA and V_O ≤ 0.8 V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.
 - Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.
 - 7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.

electrical characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = 0$, $V_{IC} = 0$, $R_S = 0$, pin 1 at 0 V, output at pin 7 (unless otherwise noted)

		TEST CONDITIONS	-+		LT1011	Y		T1011/	1	UNIT
	PARAMETER	TEST CONDITIONS	TA [†]	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
.,	1	D 5010 0 Note 5	25°C			2			0.75	mV
VIO	Input offset voltage	R _S ≤ 50 kΩ, See Note 5	Full range			3			1.5	1110
	land effect evenest	See Note 8	25°C		0.2	4		0.2	3	nA
IO	Input offset current	See Note 8	Full range			6			5	nA
	facilities armost	See Note 9	25°C		25	65		20	35	nA
IB	Input bias current	See Note 8	Full range			80			50	104
IIL(S)	Low-level strobe current (See Note 7)		25°C			-500			-500	μА
				0.5			0.5			
VICR	Common-mode input voltage range		Full range	to			to			٧
	voitage range			3			3			
AVD	Large-signal differential voltage amplification	$R_L = 0.5 \text{ k}\Omega \text{ to V}_{CC+},$ VO = 0.5 V to 4.5 V	25°C	50	300		50	300		V/mV
	Law L	$V_{ID} = -5 \text{ mV}, I_{OL} = 8 \text{ mA}$	Full range			0.4			0.4	V
VOL	Low-level output voltage	$V_{ID} = -5 \text{ mV}, I_{OL} = 50 \text{ mA}$	Full range			1.5			1.5	•
1-	Output laskage surrent	$V_{ID} = 5 \text{ mV},$	25°C		0.2	10		0.2	10	nA
Ю	Output leakage current	VO = 50 V (40 V for LT1011C)	Full range			500			500	104
ICC+	Supply current from V _{CC+}		25°C		3.2	4		3.2	4	mA
ICC-	Supply current from VCC-		25°C		-1.7	-2.5		-1.7	-2.5	mA

[†] Full range is -55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

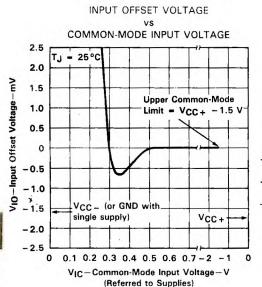
- NOTES: 6. Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.
 - 7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.
 - 8. These specifications apply for all single-supply voltages from 5 V to 30 V for the entire input voltage range, and for both high and low output states. The high state is I_{OH} ≥ 100 µA and V_O ≥ (V_{CC+} − 1 V). The low state is I_{OL} ≤ 8 mA and V_O ≤ 0.8 V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

switching characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = 0$, pin 1 at 0 V, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		LT1011			LT1011A			UNIT
PAHAMETER				MIN	TYP	MAX	MIN	TYP	MAX	UNII
Output response time	RC =	1 to 5 V, CL = 5 pF,	· · Note 9		150	250		150	250	ns

NOTE 9: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS†



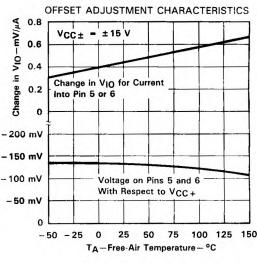


FIGURE 1

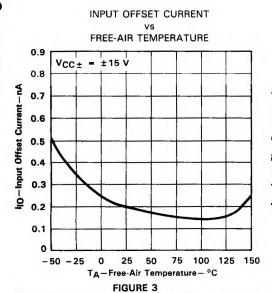


FIGURE 2

LT1011

INPUT BIAS CURRENT

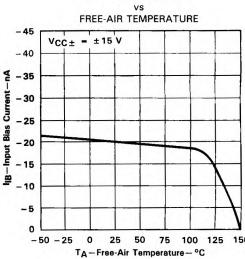
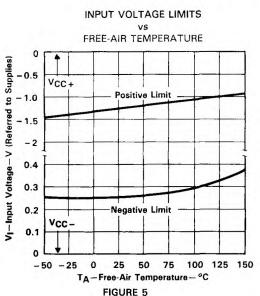


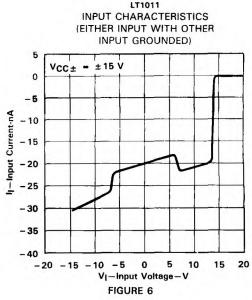
FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

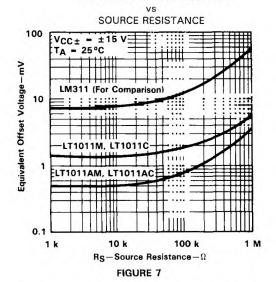


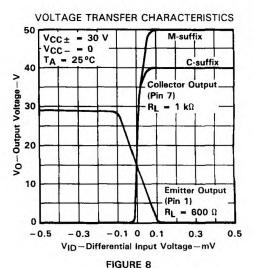
TYPICAL CHARACTERISTICS[†]





EQUIVALENT OFFSET VOLTAGE



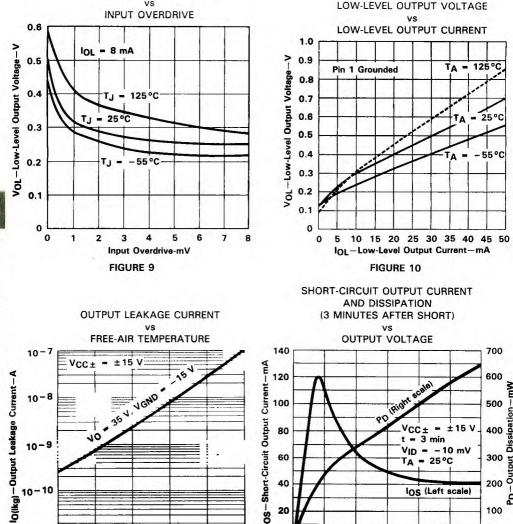


[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



LOW-LEVEL OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS[†]



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

125

105



40

20

0

0

200

100

0

15

los (Left scale)

Vo-Output Voltage-V

FIGURE 12

10-10

10-11

25

45

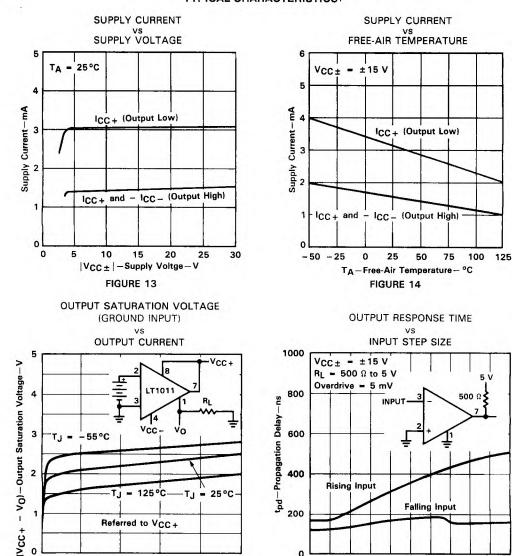
65

FIGURE 11

TA-Free-Air Temperature - °C

85

TYPICAL CHARACTERISTICS[†]



50

25°C

40

- 125°C

30

Referred to VCC+

IO-Output Current-mA

FIGURE 15

20

0

10



Rising Input

2 1

3

200

0

0

Falling Input

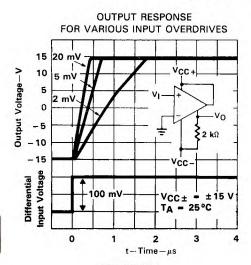
5 6 7 8 9 10

Input Step-V

FIGURE 16

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



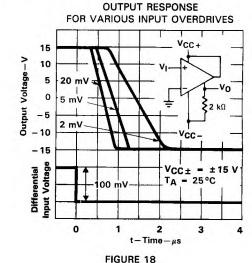
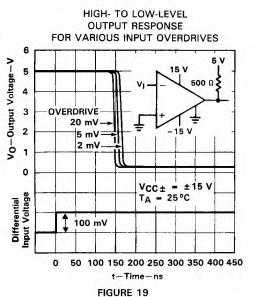
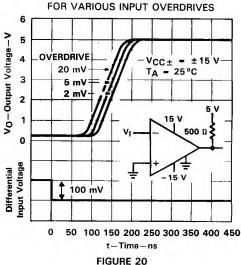


FIGURE 17



LOW- TO HIGH-LEVEL
OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES



preventing oscillation problems

Oscillation problems in comparators are often caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true for comparators with high gain and wide bandwidth, like the LT1011 (GBW ≥ 10 GHz), that are designed for fast switching with millivolt input signal levels. Because oscillation problems tend to occur at frequencies around 5 MHz, where the LT1011 has a gain of approximately 2 V/mV, attenuation of output signals must be at least 2000:1 at 5 MHz as measured at the inputs. If the source impedance is 1 kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000)(1 kΩ) = 2 MΩ, or less than 2 pF. The actual inter-lead capacitance between input and output pins on the LT1011 is less than 0.002 pF when cut to mounting length for printed circuit boards. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding.

Additional steps to prevent oscillation problems are:

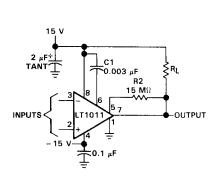
- Bypass the strobe/balance pins with a 0.01-μF capacitor connected from pin 5 to pin 6 to eliminate stray capacitive feedback from the output to the balance pins. The balance pins are nearly as sensitive to stray capacitive feedback as the inputs.
- Bypass the negative supply (pin 4) with a 0.1-μF ceramic capacitor close to the comparator. A 0.1-μF capacitor can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2-μF solid tantalum bypass capacitor.
- 3. Bypass any slow-moving or dc input with a capacitor (≥ 0.01 µF) close to the comparator to reduce high-frequency source impedance.
- 4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input, bypass it with a capacitor to balance source impedances for dc accuracy. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5-kΩ imbalance, for example, creates only 0.25-mV offset.
- 5. Use hysteresis, which consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either ac or dc. An ac hysteresis technique does not shift the apparent offset voltage of the comparator but requires a minimum input signal slew rate to be effective. A dc hysteresis technique works for all input slew rates but creates a shift in offset voltage dependent on the previous condition of the input signal.

The circuit shown in Figure 21 is an excellent compromise between ac and dc hysteresis. The 0.003-µF capacitor from pin 6 to pin 8 generates ac hysteresis by slightly shifting the voltage on the balance pins; both pins move about 4 mV depending on the state of the output. If pin 6 is bypassed, a level of ac hysteresis is created that is sufficient to switch the output at a speed near the comparator's maximum speed.

A small amount of dc hysteresis is also used to prevent problems due to low values of input slew rate. The sensitivity of the balance pins to current is about 0.5-mV input referred offset for each microampere of balance pin current. The 15-M Ω resistor tied from output to pin 5 generates 0.5-mV dc hysteresis.

The circuit is especially useful for general-purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low-frequency input signals in the millivolt range. The combination of ac and dc hysteresis creates clean oscillation-free switching with very small input errors. The curve in Figure 22 plots input referred error versus switching frequency for the circuit shown in Figure 21. Note that at low frequencies, the error is simply the dc hysteresis, while at high frequencies, an additional error is created by the ac hysteresis. The high-frequency error can be reduced by reducing CH, but lower values may not provide clean switching with very low slew-rate input signals.





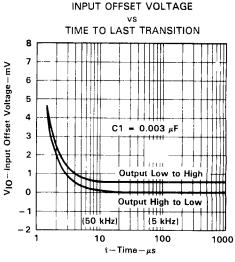
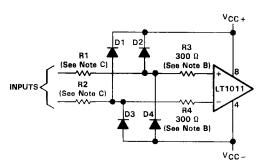


FIGURE 21. COMPARATOR WITH HYSTERESIS

FIGURE 22

input protection

The inputs to the LT1011 are particularly suited to general-purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40 V above the negative supply, independent of the positive supply voltage. Internal forward biased diodes conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1 mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used, as shown in Figure 23.



NOTES: A. D1-D4 1N4148.

B. May be eliminated for fault current ≤ 1 mA.

C. Select according to allowable fault current and power dissipation.

FIGURE 23. LIMITING FAULT INPUT CURRENTS



The input resistors should limit fault current to a value between 0.1 mA and 20 mA. Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. Lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1-D4.

R3 and R4 limit input current to the LT1011 to less than 1 mA when the input signals are held below V_{CC}—. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1 mA.

input slew rate limitations

In the LT1011, step size is important because the slew rate of internal nodes increases response time for input step sizes larger than 1 V. For example, at 5-V step size, response time increases from 150 ns to 360 ns (see Figure 16). If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. The maximum suggested common-mode slew rate is $10 \text{ V/}\mu\text{s}$.

strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an off state, giving a high output at the collector (pin 7). Currents as low as $-250 \,\mu\text{A}$ may cause strobing, but when the strobe current is low, strobe delay increases to between 200 ns and 300 ns. If strobe current is increased to $-3 \, \text{mA}$, strobe delay drops to about 60 ns. When the strobe current is 0, the voltage at the strobe pin is approximately 150 mV below VCC+; when the strobe current is increased to $-3 \, \text{mA}$, the strobe pin voltage is approximately 2 V below VCC+. Do not ground the strobe pin; it must be current driven.

Figure 24 shows a typical strobe circuit. Note that there is no bypass capacitor between pins 5 and 6, which maximizes strobe speed but leaves the comparator more sensitive to oscillation problems for slow, low-level inputs. A 1-pF capacitor between the output and pin 5 greatly reduces oscillation problems without reducing strobe speed.

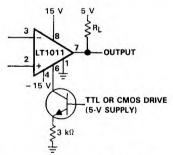


FIGURE 24. TYPICAL STROBE CIRCUIT

Placing a resistor from the output to pin 5 adds dc hysteresis. See step number 5 under "preventing oscillation problems."

The pin that is used for strobing (pin 6) is also one of the offset adjustment pins. Current into or out of pin 6 must be kept very low ($<0.2 \mu A$) when not strobing to prevent input offset voltage shifts.

output transistor

When the LT1011 output transistor is in the off state, negligible current flows into or out of the collector or emitter. The equivalent circuit is shown in Figure 25.



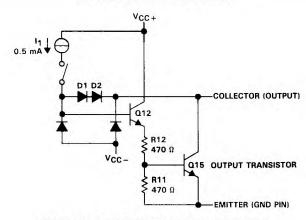


FIGURE 25. OUTPUT TRANSISTOR CIRCUITRY

output transistor (continued)

In the off state, I1 is switched off and both Q12 and Q15 turn off. The collector of Q15 can then be held above VCC- without conducting current. The maximum voltage above VCC- is 50 V for the LT1011 and 40 V for the LT1011C (these maximum voltages may exceed VCC+). The emitter can be held at any voltage between VCC- and VCC+ as long as the voltage is negative with respect to the collector.

In the on state, I₁ is connected, which turns on both Q12 and Q15. Diodes D1 and D2 prevent deep saturation of Q15 to improve speed and also limit the drive current of Q12. The R11/R12 divider sets the saturation voltage of Q15 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between VCC- and VCC+, which allows the remaining pin to drive the load. In typical applications, the emitter is connected to VCC- or ground, and the collector drives a load tied to VCC+ or a separate positive supply.

When the emitter is used as the output, the collector is typically tied to VCC+, and the load is connected to ground or VCC -. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "-" input designations must be reversed. When the collector is tied to VCC+, the voltage at the emitter in the one state is about 2 V below VCC+.

input signal range

The input voltage range of the LT1011 is typically 300 mV above the negative supply and 1.5 V below the positive supply, independent of the actual supply voltages. This is the input voltage range over which the output will respond correctly when a voltage within the range is applied to one input and a higher or lower signal is applied to the other input. If one input is inside the range and one is outside, the output will be correct. If both inputs are outside the range, in opposite directions, the output will still be correct. If, however, both inputs are outside the range in the same direction, the output will not respond to the differential input; it will remain unconditionally off.



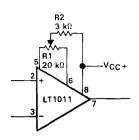
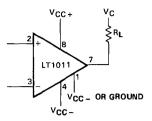


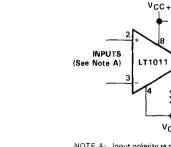
FIGURE 26. OFFSET BALANCING

LT1011



NOTE: Vc can be greater or less than Vcc+.

FIGURE 28. DRIVING LOAD REFERENCED TO POSITIVE SUPPLY



NOTE A: Input polarity is reversed when using Pin 1 for output.

Vcc-

NOTE: Do not ground strobe pin

1 kΩ

STROBE

FIGURE 27. STROBING

FIGURE 29. DRIVING LOAD REFERENCED TO NEGATIVE SUPPLY

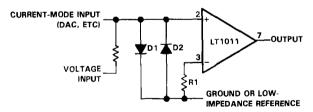
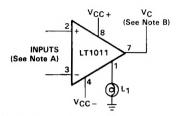


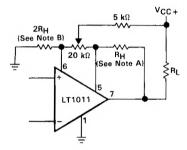
FIGURE 30. USING CLAMP DIODES TO IMPROVE FREQUENCY RESPONSE (See Figure 16)



NOTES: A. Input polarity is reversed when using Pin 1 for output.

B. V_C may be any voltage above V_{CC} -. Pin 1 swings to within approximately 2 V of VCC+.

FIGURE 31. DRIVING LOAD REFERENCED TO GROUND



NOTES: A. Hysteresis is approximately 0.45 mV/µA change in current in RH.

B. This resistor causes hysteresis to be centered around

FIGURE 32. COMBINING OFFSET ADJUSTMENT AND HYSTERESIS

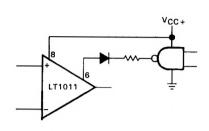


FIGURE 33. DIRECT STROBE DRIVE WHEN CMOS LOGIC USES SAME VCC+ SUPPLY AS LT1011 (Not applicable for TTL logic)

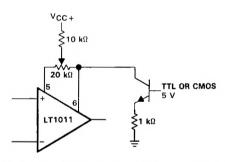
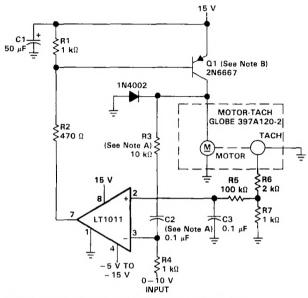


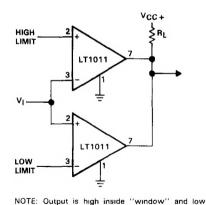
FIGURE 34. COMBINING OFFSET ADJUSTMENT AND STROBE



NOTES: A. R3/C2 determines oscillation frequency of controller.

B. Q1 operates in switch mode.

FIGURE 35. HIGH-EFFICIENCY MOTOR SPEED CONTROLLER



above high limit or below low limit.

FIGURE 36. WINDOW DETECTOR

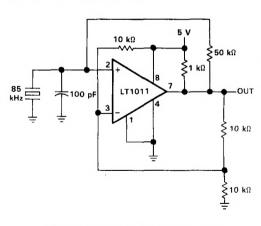
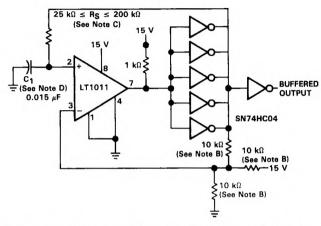
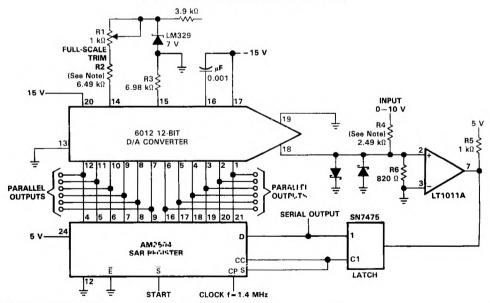


FIGURE 37. CRYSTAL OSCILLATOR



- NOTES: A. Low drift and accurate frequency are obtained because this configuration rejects effects due to input offset voltage and input bias current of the comparator.
 - B. 1% metal film.
 - C. R_S = TRW type MTR-5/ + 120 ppm/ $^{\circ}$ C.
 - D. $C_1 = 0.015 \,\mu\text{F} = \text{polystyrene} : 120 \,\text{ppm/}\,^{\circ}\text{C} \pm 30 \,\text{ppm}$ WESCO type 32-P.
 - E. Comparator contributes ≤ 10 ppm/°C drift for frequencies below 10 kHz.

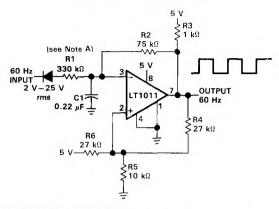
FIGURE 38. LOW-DRIFT R/C OSCILLATOR



NOTE: R2 and R4 should TC track.

FIGURE 39. 10-µs 12-BIT A-D CONVERTER

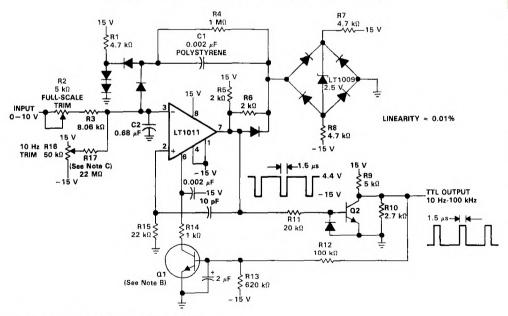




NOTES: A. Increase R1 for larger input voltages.

B. LT1011 self-oscillates at approximately 60 Hz, thereby "locking" onto incoming line signal.

FIGURE 40. NOISE-IMMUNE 60-Hz LINE SYNCHRONIZATION

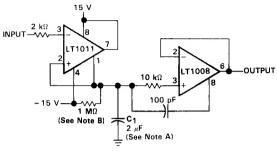


NOTES: A. All diodes 1N4148, transistors 2N3904.

- B. Used only to guarantee start-up.
- C. R17 may be increased for better 10-Hz trim resolution.

FIGURE 41. 10-Hz TO 100-kHz VOLTAGE-TO-FREQUENCY CONVERTER

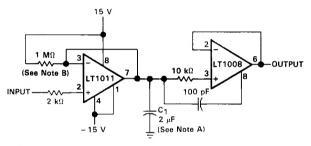




NOTES: A. Mylar

B. Set for required reset time constant.

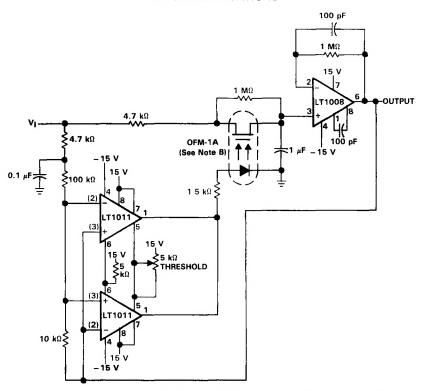
FIGURE 42. POSITIVE PEAK DETECTOR



NOTES: A. Mylar

B. Select for required reset time constant.

FIGURE 43. NEGATIVE PEAK DETECTOR



NOTES: A. The comparators drive the opto-coupled FET "on" when the difference between the output and the input exceeds threshold. When the output approaches the input, the FET turns "off" and low-pass filtering occurs.

B. From Theta-J Corporation, Woburn, Massachusetts.

FIGURE 44. FAST-SETTLING FILTER

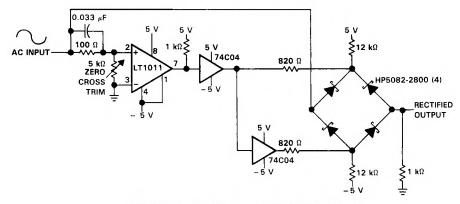
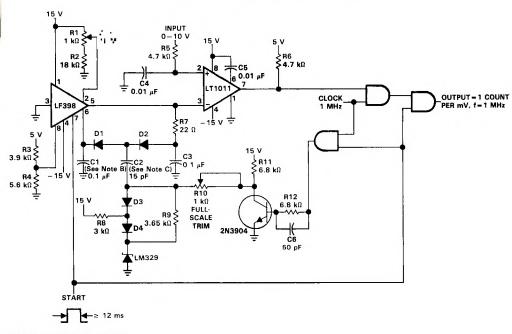


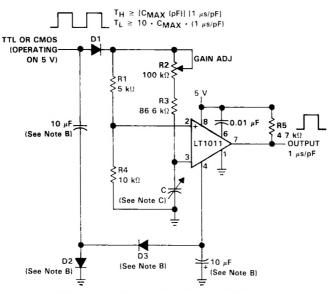
FIGURE 45. 100-kHz PRECISION RECTIFIER



NOTES: A. All diodes 1N4148

- B. Polystyrene
- C. NPO

FIGURE 46. 4-DIGIT (10,000-COUNT) A-D CONVERTER



- NOTES: A. PW = (R2 + R3) (C) [(R1 + R4)/R1]. The input capacitance of the LT1011 is approximately 6 pF. This is an offset term.
 - B. These components may be eliminated if negative supply is available (-1 V to -15 V).
 - C. Typical two sections of 365-pF variable capacitor when used as shaft-angle indication.

FIGURE 47. CAPACITANCE-TO-PULSE-WIDTH CONVERTER

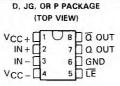
LT1016 ULTRA-FAST PRECISION LATCHED COMPARATOR

D3242, MAY 1988-REVISED MARCH 1989

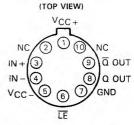
- Ultra-Fast . . . 10 ns Typ tod
- Operates from Single 5-V or Dual ±5-V Supply
- Complementary TTL Outputs
- Low Input Offset Voltage . . . 0.8 mV or 1 mV Typ
- No Minimum Input Slew Rate Requirement
- No Supply Current Spiking
- Output Latch

description

The LT1016 is an ultra-fast comparator specifically designed to interface directly to TTL logic while operating from either a dual $\pm\,5\text{-V}$ supply or a single 5-V supply. The LT1016 offers tight offset voltage specifications and high gain for precision applications. Matched complementary outputs further extend the versatility of the LT1016.



L PACKAGE



NC-No internal connection

All leads of the L package are electrically insulated from the case.

case.

The LT1016 features a unique output stage that provides active drive in both directions for maximum speed into TTL-logic or passive loads yet does not exhibit the large current spikes normally found in totem-pole output stages. This eliminates the need for a minimum input slew rate typical of other fast comparators. The LT1016's ability to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is at a low level.

The LT1016 has a true latch for retaining input data at the outputs. The outputs remain latched as long as the latch enable input $\overline{\text{LE}}$ is high. Quiescent negative supply current is only 3 mA, about ten times lower than competitive units. This feature reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

The LT1016M is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$. The LT1016C is characterized for operation from 0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$.

AVAILABLE OPTIONS

	PACKAGE							
TA	SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN	PLASTIC DIP				
0°C to 70°C	LT1016CD	LT1016CJG	LT1016CL	LT1016CP				
- 55°C to 125°C		LT1016MJG	LT1016ML					

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LT1016CDR).



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC+ (see Note 1)	
Supply voltage, VCC	7 V
Differential input voltage (see Note 2)	±5 V
Input voltage (either input)	V _{CC±}
Latch enable input voltage	VCC±
Output current, IO	± 20 mA
Operating free-air temperature range: LT1016M	55°C to 125°C
LT1016C	0°C to 70°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 second	is: D or P package 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 second	is: JG package 300°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 second	is: L package 300°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. The output may be shorted to ground or to either power supply.

recommended operating conditions

			LT1016	VI	LT1016C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Supply voltage, V _{CC+}			•	5			5	٧
Supply voltage, V _{CC} -				-5			-5	V
I and the second	V _{CC±} = ±15 V	-3.75		3.5	-3.75		3.5	V
Input voltage, V _I	$V_{CC+} = 5 \text{ V}, V_{CC-} = 0$	1.25		3.5	1.25		1.25	٧
Operating free-air temperature, TA		- 55		125	0		70	°C

LT1016 ULTRA-FAST PRECISION LATCHED COMPARATOR

electrical characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $V_{O(Q)} = 1.4 \text{ V}$, $\overline{\text{LE}}$ at 0 V (unless otherwise noted)

	DADAMETED	TEST CONDITIONS	TAT	LT1016M		LT1016C			UNIT	
	PARAMETER	TEST CONDITIONS	'A'	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
14	Input offset voltage	B 100.0	25°C		0.8	2		1	3	
VIO	(see Note 4)	$R_S \leq 100 \Omega$	Full range			3			3.5	mV
^α Vιο	Average temperature coefficient of input offset voltage		Full range		4			4		μV/°C
lio.	input offset current		25°C		0.3	1		0.3	1	μА
lo lo	(see Note 4)		Full range			1.3			1.3	μΑ
l _{IB}	Input bias current	V _O = 1.4 V	25°C		5	10		5	10	μА
אוי	(see Note 5)	V0 = 1:4 V	Full range			13	SALT		13	μΑ
V	Common-mode input	Dual supply	Full range	-3.75 to 3.5			-3.75 to 3.5			V
VICR	voltage range	Single supply	Full range	1.25 to 3.5			1.25 to 3.5			·
.,		LE high	Full range	2			2			v
VI	Input voltage	LE low	Full range			0.8			0.8	\ \
Vari	High-level	$V_{CC+} \le 4.6 \text{ V, I}_{O} = 1 \text{ mA}$	Full range	2.7			2.7			V
VOH	output voltage	$V_{CC+} \le 4.6 \text{ V, I}_{O} = 10 \text{ mA}$	ruii range	2.4	-		2.4		4.1	
Va	Low-level	lo = 4 mA	Full range			0.5			0.5	v
VOL	output voltage	I _O = 10 mA	25°C		0.4			0.4		
AVD	Small-signal differential voltage amplification	V _O = 1 V to 2 V	25°C	1400	3000		1400	3000		V/V
CMRR	Common-mode rejection ratio	$V_{IC} = -3.75 \text{ V to } 3.5 \text{ V}$	Full range	80			80			dB
leas and	Supply voltage	Positive supply, $V_{CC+} = 4.6 \text{ V to 5.4 V}$	Full range	60			60			4D
ksvr	rejection ratio	Negative supply, V _{CC} = 2 V to 7 V	rus lange	80			80			dB
lcc+	Supply current from V _{CC+}		Full range			35			35	mA
lcc-	Supply current from V _{CC} -		Full range			5			5	mA
fj	Latch pin input current		Full range			500			500	μΑ

[†]Full range is -55°C to 125°C for the LT1016M. Full range is 0°C to 70°C for the LT1016C.

NOTES: 4. Input offset voltage is defined as the average of the two voltages measured by forcing first one output and then the other to 1.4 V. Input offset current is defined in an analogous way.

^{5.} Input bias current is defined as the average of the two input currents.

switching characteristics, $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $\overline{\text{LE}}$ at 0 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TA [†]	MIN	TYP	MAX	UNIT
		$\Delta V_1 = 100 \text{ mV}, 5\text{-mV overdrive},$	25°C		10	14	
	December delegation	See Note 6	Full range			16	
tpd	Propagation delay time	$\Delta V_{\parallel} = 100 \text{ mV}, 20\text{-mV} \text{ overdrive},$	25°C		10	14	ns
		See Note 6	Full range			16	
Δ _{tpd}	Differential propagation delay	$\Delta V_1 = 100 \text{ mV}, 5\text{-mV} \text{ overdrive},$ See Note 6	25°C			3	ns
	Latch minimum setup time		25°C		2		ns

†Full range is -55°C to 125°C for the LT1016M. Full range is 0°C to 70°C for the LT1016C.

NOTE 6: tpd and Atpd cannot be measured in automatic-handling test equipment with low values of overdrive. The LT1016 is tested with a 1-V step and 500-mV overdrive. Correlation testing indicates that t_{pd} and Δt_{pd} limits shown can be met with this test. For low overdrive conditions, VIO is added to the overdrive.



Single Supply or Dual Supplies

- Wide Range of Supply Voltage 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current 3 to 5 nA Typ
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

- (то	P VI	EΝ	/)
NC	1	U	8	Пис
IN - [2		7	Vcc
IN +	3		6	
GND	4		5	NC

D. JG. OR P PACKAGE

NC-No internal connection

AVAILABLE OPTIONS

		PACE AGE					
TA	V _{IO} MAX at 25°C	SMALL OUTLINE (D)	CLRAMIC. DIP (JG)	PLASTIC DIP (P)			
0°C to 70°C	5 mV	TL331CD	TL331CJG	TL331CF			
- 25°C to 85°C	5 mV	TL331ID	TL331IJG	TL331IP			

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL331CDR)

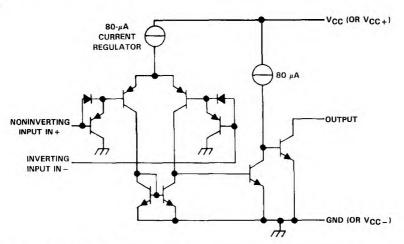
description

The TL331 is a voltage comparator that is designed to operate from a single power supply

over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 36 V and pin 7 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage.

The TL331I is characterized for operation from $-25\,^{\circ}\text{C}$ to $85\,^{\circ}\text{C}$. The TL331C is characterized for operation from $0\,^{\circ}\text{C}$ to $70\,^{\circ}\text{C}$.

schematic



Current values shown are nominal.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Differential input voltage (see Note 2)
Input voltage range (either input)
Output voltage
Output current
Duration of output short-circuit to ground (see Note 3) unlimited
Continuous total dissipation See Dissipation Rating Table
Operating free-air temperature range: TL331I
TL331C 0°C to 70°C
Storage temperature range
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds; D or P package 260 °C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. Short circuits from the output to VCC can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	TA ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING
D	• mW	5.8 mW/°C	464 mW	, . mM
JG	680 mW	6.6 mW/°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		TLS	331I TL331C		31C		
		MIN	MAX	MIN	MAX	UNIT	
Supply voltage, VCC		5	35	5	30	٧	
	V _{CC} = 5 V	0	3	0	3	1,,	
Common-mode input voltage, VIC	V _{CC} = 30 V	0	28	0	28	V	
Operating free-air temperature, TA		-25	85	0	70	°C	

electrical characteristics at specified free-air temperature, VCC = 5 V (unless otherwise noted)

		TEST CONDITIONS†			1	L331		T	L3310	;	UNIT
	PARAMETER	IESI	CONDITIONS	200	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
		V _{CC} = 5 V to 3	30 V,	25°C		2	5		2	5	
VIO	Input offset voltage	VIC = VICR mir	n, $V_0 = 1.4 \text{ V}$	Enl, tavde			9			9	mV
				2.		3	25		5	50	nA
lo	input offset current	$V_0 = 1.4 \text{ V}$	VO = 1.4 V							150	nA.
	TOWNS CONCEDED		2			- 25			- 25		
IB	Input bias current			Full range			- 300				nA
			05.00	0 to		- 111	0 to				
	Common-mode input		00.14	25°C	VCC-1.5	5		VCC - 1.	5		v
VICR	voltage range	$V_{CC} = 5 \text{ V to}$	30 V	Full range	0 to			0 to			7 "
					VCC-2			Vcc-2			
AVD	Large-signal differential voltage amplification	$V_{CC} = 15 \text{ V},$ $V_{O} = 1.4 \text{ V to}$ $R_{L} = 15 \text{ k}\Omega \text{ to}$		25°C		200			200		V/mV
	High-level		V _{OH} = 5 V	25°C		0.1			0.1		nA
IOH	output current	$V_{ID} = 1 V$	V _{OH} = 30 V	Full range			1			1	μΑ
2027	Low-level	110000000000000000000000000000000000000	E 4 E 4 E 5 A 5 A 5 A 5	25°C		150	- i		150	400	
VOL	output voltage	$V_{ID} = -1 V$	$l_{OL} = 4 \text{ mA}$	Full range						700	mV
lOL	Low-level output current	V _{ID} = -1 V,	V _{OL} = 1.5 V	25°C	6			6			mA
Icc	Supply current	$V_0 = 2.5 V$	No load	25°C		0.5	0.8	7	0.5	0.8	mA

[†] Full range (MIN to MAX) for the TL331I is -25°C to 85°C and for the TL331C is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, VCC = 5 V, TA = 25 °C

PARAMETER	TEST C	CONDITIONS	MIN	TYP	MAX	UNIT
	R _L connected to 5 V through 5.1 kΩ,	nV input step with 5-mV overdrive		1.3	10.00	
Response time	C _L = 15 pF, [‡] See Note 4	TTL-level input step		0.3		μς

[‡]C_L includes probe and jig capacitance.
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

1988

TL514M DUAL DIFFERENTIAL COMPARATOR WITH STROBE

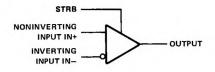
- Fast Response Times
- High Differential Voltage Amplification
- Low Offset Characteristics
- Outputs Compatible with Most TTL Circuits

description

The TL514 is an improved version of the TL720 dual high-speed voltage comparator. When compared with the TL720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characteristics, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

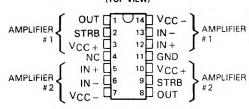
These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The TL514M is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to $125\,^{\circ}\text{C}$.

symbol (each comparator)

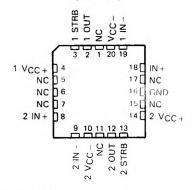


J OR W PACKAGE (TOP VIEW)

D999, OCT · :977-RE.

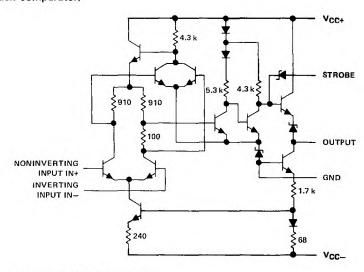


FK CHIP CARRIER (TOP VIEW)



NC - No internal connection

schematic (each comparator)



Resistor values shown are nominal in ohms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage VCC+ (see Note 1)
Supply voltage VCC – (see Note 1)
Differential input voltage (see Note 2) ±5 V
Input voltage (any input, see Note 1)
Strobe voltage (see Note 1)
Peak output current (t _W ≤1 s)
Continuous total dissipation (either comparator or both together) See Dissipation Rating Table
Operating free-air temperature range
Storage temperature range65°C to 150°C
Case temperature for 60 seconds: FK package
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package 300 °C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C PO∵FR RATING	DERATING FACT: IN	DERATE Alicis E TA	TA = 125°C POWLH RATING
FK	mW	11 0 r ' 3		mW
J	600 mW	11.0 mW/°C	95°C	275 mW
W	600 mW	8.0 mW/°C	75 °C	200 mW



DUAL DIFFERENTIAL COMPARATOR WITH STROBE

W	PARAMETER	TEST CONDIT	IONS†	MIN	TYP	MAX	UNIT
.,		$R_S \leq 20 \Omega$,	25 °C		0.6	2	
VIO	Input offset voltage	See Note 4	-55°C to 125°C	1		3	m∨
C. N.	Average temperature coefficient	$R_S = 50 \Omega$,	-55°C to 25°C		3	10	
ανιο	of input offset voltage	See Note 4	25°C to 125°C		3	10	μV/°C
			25°C		0.75	3	
lio	Input offset current	See Note 4	−55 °C		1.8	7	μΑ
			125 °C		0.25	3	446
	Average temperature coefficient	See Note 4	-55°C to 25°C		15	75	nA/°C
αIIO	of input offset current	See Note 4	25°C to 125°C		5	25	nA/*C
C.a.	Inches bloom and the second	Can Nasa 4	25 °C		7	15	
IB	Input bias current	See Note 4	- 55°C		12	25	μΑ
IH(S)	High-level strobe current	$V_{(strobe)} = 5 V,$ $V_{ID} = -5 \text{ mV}$	25°C			± 100	μΑ
I _{IL(S)}	Low-level strobe current	$V_{(strobe)} = -100 \text{ mV},$ $V_{ID} = 5 \text{ mV}$	25°C		- 1	- 2.5	mA
VICR	Common-mode input	V _{CC} = -7 V	-55°C to 125°C	±5			٧
VID	· rential input voltage range		-55°C to 125°C	±5			٧
	Large-signal differential	No load,	25 °C	12.5	33		177
AVD	voltage amplification	$V_0 = 0 \text{ to } 2.5 \text{ V}$	-55°C to 1. · C	10			V/m\
		V _{ID} = 5 mV I _{OH} = 0	-55°C to 125°C		45	5	
∨он	High-level output voltage	V _{ID} = 5 mV, I _{OH} = -5 mA	-55°C to 125°C	2.5	3.6 §		٧
		V _{ID} = -5 mV, I _{OL} = 0	-55°C to 125°C	-1	-0.5§	o‡	V
VOL	Low-level output voltage	V _(strobe) = 0.3 V, V _{ID} = 5 mV, I _{OL} = 0	-55°C to 125°C	-1		0‡	٧
			25 °C	2	2.4		
OL	Low-level output current	$V_{ID} = -5 \text{ mV},$	-55°C	1	2.3	. 1	mA
77		$V_0 = 0$	125°C	0.5	2.3		
o	Output resistance	V ₀ = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	Rs ≤ 200 Ω	-55°C to 125°C	80	100§		dB
	Supply current from V _{CC+} ¶	<u> </u>	-55°C to 125°C		115	18	mA
		$V_{ID} = -5 \text{ mV},$	*				10000
CC-	Supply current from V _{CC} -	No load	-55°C to 125°C		-75	- 14	mA

electrical characteristics at specified free-air temperature Vcc . = 12 V Vcc . = -6 V

-55°C to 125°C

1805

300

mW

Total power dissipation

PD

[†] Unless otherwise noted, all characteristics are measured with the strobe open.

[‡] The algebraic convention, where the most-positive (least-negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.

 $^{^{5}}$ These typical values are at $T_{A} = 25$ °C.

Supply current and power dissipation limits apply for both comparators operating simultaneously.

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: Vo = 1.8 V at TA = -55°C, VO = 1.4 V at TA = 25°C, and VO = 1 V at TA = 125°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits this comparator is intended to drive.

DUAL DIFFERENTIAL COMPARATOR WITH STROBE

switching characteristics, VCC+ = 12 V, VCC- = -6 V, TA = 25°C

PARAMETER		TEST CONDITIO	NS	MIN	TYP	MAX	UNIT
Response time	R _L = ∞	C _L = 5 pF,	See Note 5		30	80	ns
Strobe release time	R _L = ∞	C _L = 5 pF,	See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.

6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4-V level.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL **VOLTAGE AMPLIFICATION**

VS FREE-AIR TEMPERATURE AVD-Differential Voltage Amplification-V/mV 60 VCC+ = 12 V $V_{CC-} = -6 V$ 50 Vo = 0 to 2.5 V No load 40 30 20 10 -50 -250 25 -75 50 75 100 125 TA-Free-Air Temperature-°C

LARGE-SIGNAL DIFFERENTIAL **VOLTAGE AMPLIFICATION**

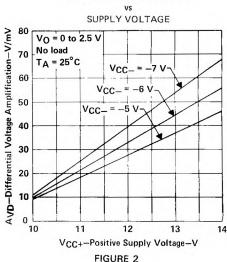
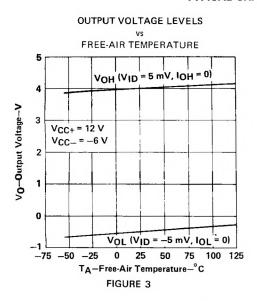
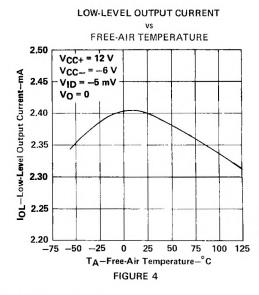
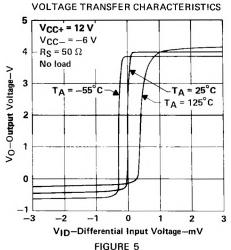
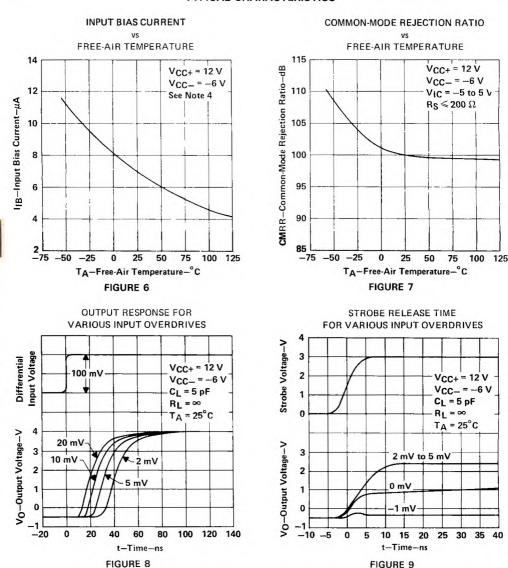


FIGURE 1



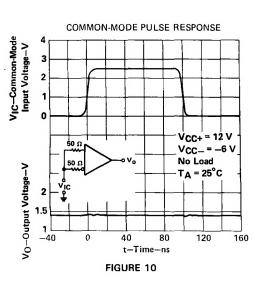


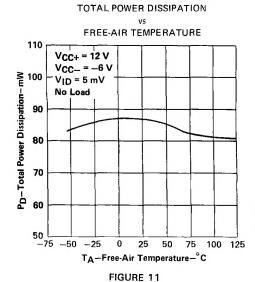




NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.8 V at $T_A = -55$ °C, $V_O = 1.4$ V at $T_A = 25$ °C, and $V_O = 1$ V at $T_A = 125$ °C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits this comparator is intended to drive.







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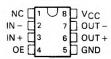
- 0 to 5 V Common-Mode input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- **Enable Capability**
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

description

The TL712 is a high-speed comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary 3-state TTLcompatible logic outputs with symmetrical switching characteristics. When the output enable, OE, is low, both outputs are in the highimpedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

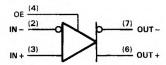
The TL712 is characterized for operation from 0°C to 70°C.

D. JG. OR P PACKAGE (TOP VIEW)

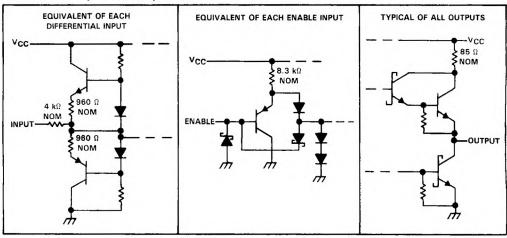


NC-No internal connection

symbol (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage, any differential input
Differential input voltage (see Note 2)
Enable input voltage
Low-level output current
Operating free-air temperature range
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.

2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN NOM MAX	UNIT
Supply voltage, VCC	4.75 5 5.2	5 V
Common-mode input voltage, VIC	±1!	5 V
High-level output current, IOH		mA
Low-level output current, IOL	10	mA
Operating free-air temperature, TA	0 70	°C

electrical characteristics at VCC = 5 V, TA = 25°C

	PARAM': IFR	TEST CONDITIONS	2017	TYP	MAX	UNIT
VΤ	Threshold voltage (v + and V -)	VICR = 0 to 5 V			1	IIIV
Vhys	Hysteresis (VT+ - VT-)			5	=:	mV
Voн	High-level output voltage	$V_{ID} = 100 \text{ mV}, I_{OH} = -1 \text{ mA}$	2.7	3.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV}, I_{OL} = 16 \text{ mA}$		0.4	0.5	V
loz	Off-state output current	V _O = 2.4 V			-20	μΑ
l _l	Enable current	V _I = 5.5 V			100	μΑ
ΊΗ	High-level enable current	$V_{IH} = 2.7 V$			20	μΑ
IIL	Low-level enable current	V _{IL} = 0.4 V	10		-360	μΑ
rį	Differential input resistance		4			kΩ
ro	Output resistance				100	Ω
los	Short-circuit output current		-15		-85	mA
lcc	Supply current	V _{ID} = 0, No load		17	20	mA

[†] The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	I : · I · · ! · I .TIONS	MIN TYP	MAX	UNIT
tPLH	Propagation delay time, low-to-high-level output	Til load (see Figure 1),	25		ns
tPHL.	Propagation delay time, high-to-low-level output	See Note 3	25		ns

NOTE 3: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.



PARAMETER MEASUREMENT INFORMATION

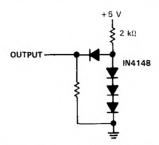
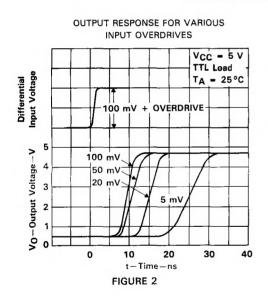
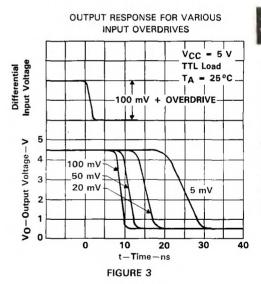


FIGURE 1. TTL OUTPUT LOAD CIRCUIT





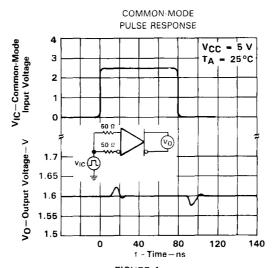
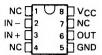


FIGURE 4

- Self-Biasing Inputs
- Hysteresis . . . 10 mV Typical
- Response Time . . . 7 ns Typical
- Maximum Operating Frequency . . . 50 MHz Typical

D OR P PACKAGE (TOP VIEW)



NC-No internal connection

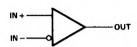
description

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

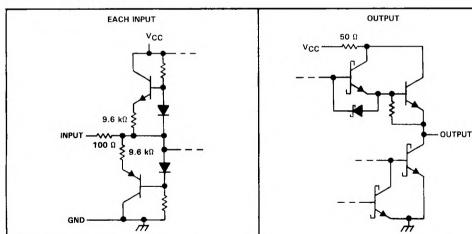
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

The TL714C is characterized for operation from 0°C to 70°C.

symbol



schematic of inputs and output



All resistor values shown are nominal.

NOTES: 1. All voltage values, except for differential voltage, are with respect to the network ground.

2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	TA ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING
D	nW	5.8 mW/°C	64°C	464 mW
P	500 mW	N/A	N/A	500 mW

recommended operating conditions

PARAMETER	MIN MAX	UNIT
Supply voltage, V _{CC}	4.75 5.25	V
	1.4	
mmon-mode input voltage, V _{IC}	to	V
	V _{CC} -1.4	
High-level output current, IOH	-1	mA
Low-level output current, IOL	16	mA
Operating free-air temperature, TA	0 70	°C

electrical characteristics over free-air operating temperature range, V_{CC} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
٧T	Threshold voltage	V _{IC} = 1.4 V to 3.6 V	1		±20	m۷
Vhys	Hysteresis (V _{T+} - V _{T-})		2	10	20	mV
Voн	High-level output voltage	$V_{ID} = 100 \text{ mV}, I_{OH} = -1 \text{ mA}$	2.7	3.4		٧
VOL	Low-level output voltage	V _{ID} = -100 mV, I _{OL} = 16 mA		0.4	0.5	٧
los	Short-circuit output current		-15		-85	mA
ri	L I'- rential input resistance		2.9			kΩ
ro	Output resistance				100	Ω
Icc	Supply current	$V_{ID} = 0, I_{O} = 0$		7	20	mA

[†]All typical values are at T_A = 25 °C.

switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	IFST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum operating frequency	$V_{\text{ID}} = \pm 250 \text{ inV}, t_{\text{f}} = t_{\text{f}} = 4 \text{ ns},$ $C_{\text{L}} = 25 \text{ pF}, \text{ Input duty cycle} = 50\%$		50		MHz
tPLH.	Propagation delay time, low-to-high-level output	$V_{ID} = \pm 100 \text{ mV}, C_L = 25 \text{ pF},$		7	25	ns
tPHL	Propagation delay time, high-to-low-level output	See Figures 1 and 2		7	25	ns
tr	Rise time	$V_{ID} = \pm 100 \text{ mV}, C_L = 25 \text{ pF},$		4	8	ns
tf	Fall time	See Figure 3		4	8	ns



PARAMETER MEASUREMENT INFORMATION

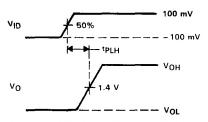


FIGURE 1. PROPAGATION DELAY TIME, LOW TO HIGH (tpLH)

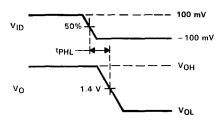


FIGURE 2. PROPAGATION DELAY TIME, HIGH TO LOW (tpHL)

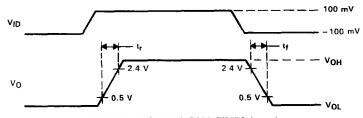


FIGURE 3. RISE AND FALL TIMES (tr, tf)

- Common-Mode Input Voltage Range 0 V to -5.2 V
- MECL III and MECL 10 000 Compatible

Operates from a -5.2-V Power Supply

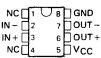
- Complementary ECL-Compatible Outputs
- Hysteresis . . . 5 mV Typ
- Response Times . . . 10 ns Typ

description

The TL721 is a high-speed voltage comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary ECL-compatible logic with symmetrical switching characteristics. The device operates from a single - 5.2-volt supply and is useful as a disk memory read-chain data comparator.

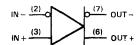
The TL721 is characterized for operation from 0°C to 70°C.

D. JG. OR P PACKAGE (TOP VIEW)



NC-No internal connection

symbol



†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	-7 V
Input voltage, any differential input ±	25 V
Differential input voltage (see Note 2) ±	25 V
Low-level output current 5	0 mA
Operating free-air temperature range	70°C
Storage temperature range65°C to 1	50°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
 - 2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN NOM MAX	UNIT
Supply voltage, V _{CC}	- 5.2	V
Common-mode input voltage, V _{IC}	±7	V
High-level output current, IOH		mA
Low-level output current, IOL	16	mA
Operating free-air temperature, TA	0 70	°C

electrical characteristics at TA = 25 °C, VCC = -5.2 V

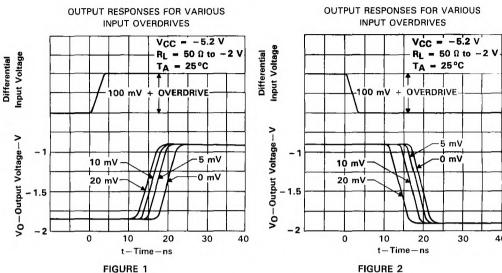
	PARAMETER	TEST CO	ONDITIONS	MIN	TYP MAX	UNIT
VT	Threshold voltage (VT+ and VT-)	VIC = VICR min		-1		mV
Vhvs	Hysteresis (VT+ - VT-)				5	mV
Voн	High-level output voltage	V _{ID} = 100 mV,	$R_L = 50 \Omega \text{ to } -2 \text{ V}$	-0.96 [†]	-0.81	٧
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	R _L = 50 Ω to -2 V	-1.85 [†]	-1.65	V
VICR	Common-mode input voltage range			0 to -5.2		v
rin	Input resistance			4		kΩ
Icc	Supply current	$V_{ID} = 0$,	No load		-13 -17	mA

[†] The algebraic convention, in which the more negative limit is designated as minimum, is used in this data sheet for input threshold and output voltage levels only.

switching characteristics at TA = 25 °C, VCC = -5.2 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	$\Delta V_{ID} = +200 \text{ mV to } -200 \text{ mV or}$		18		ns
tPHL	Propagation delay time, high-to-low-level output	$-200 \text{ mV to } +200 \text{ mV},$ $R_L = 50 \Omega \text{ to } -2 \text{ V}$		18		ns





HIGON

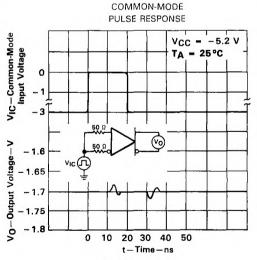


FIGURE 3

TLC339M, TLC339I, TLC339C QUADRUPLE MICROPOWER LincMOS™ COMPARATORS

D3135, DECEMBER 1986 - REVISED FEBRUARY 1989

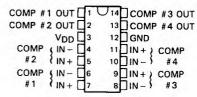
- Very Low Power . . . 200 μW Typ at 5 V
- Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation: TLC339M . . . 4 V to 16 V TLC339I . . . 3 V to 16 V TLC339C . . . 3 V to 16 V
- High Input Impedance . . . 10¹² Ω Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

description

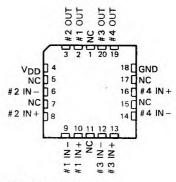
The TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias

TLC339M . . . J PACKAGE TLC339I, TLC339C . . . D, J, OR N PACKAGE (TOP VIEW)

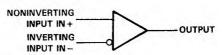


TLC339M . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

symbol (each comparator)



AVAILABLE OPTIONS

		PACKAGE					
TA	V _{IO} max at 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)		
0°C to 70°C	5 mV	TLC339CD	-	TLC339CJ	TLC339CN		
-40°C to 85°C	5 mV	TLC339ID	44	TLC339IJ	TLC339IN		
-55°C to 125°C	5 mV	-	TLC339MFK	TLC339MJ	-		

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., TLC339CDR)

. 1 V. . s a trademark of Texas Instruments Incorporated.

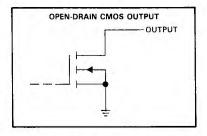


description (continued)

currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC339M is characterized for operation over the full military temperature range of -55°C to 125°C. The TLC339I is characterized for operation over the extended industrial temperature range of -40°C to 85°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)	1
Differential input voltage (see Note 2)	
Input voltage, V ₁ 0.3 V to V _{DD}	
Output voltage, VO	
Input current, II	4
Output current, Io (each output)	
Total supply current into V _{DD} terminal	
Total current out of ground terminal	4
Continuous total dissipation See Dissipation Rating Table	е
Operating free-air temperature range: TLC339M	3
TLC339I	2
TLC339C 0°C to 70°C)
Storage temperature range)
Case temperature for 60 seconds: FK package)
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260°C)
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package)

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING	T _A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	_
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC339M)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC339I & C)	1025 mW	8.2 mW/°C	656 mW	533 mW	-
N	1150 mW	9.2 mW/°C	736 mW	598 mW	



TLC339M QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4	5	16	٧
Common-mode input voltage, VIC	0		V _{DD} -1.5	٧
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	-55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDIT	ronst	MIN	TYP	MAX	UNIT
		VIC = V _{ICR} min,	25°C		1.4	5	
V _{IO}	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	55°C to 125°C			10	mV
l.a	lanut offeet current	V10 - 2 5 V	25°C		1		pΑ
lo	Input offset current	V _{IC} = 2.5 V	125°C			15	nA
220	Innut bios surrent	V 2 E V	25°C		5		pΑ
lB	Input bias current	V _{IC} = 2.5 V	125°C			30	nA
V	Common-mode input voltage range		25°C	0 to V _{DD} -1			V
VICR			-55°C to 125°C	0 to V _{DD} -1.5			
5.00	Common-mode rejection ratio	V _{IC} = V _{ICR} min	25°C		84		
CMRR			125°C		84		dB
			−55°C		84		
			25°C		85		
KSVR	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	125°C		84		dB
			-55°C	84			
V	I am land a dan disaltana	$V_{1D} = -1 V$,	25°C		300	400	
VOL	Low-level output voltage	IOL = 6 mA	125°C			800	mV
12.33	(Bab lavet autout autout	V _{ID} = 1 V,	25°C		0.8	40	nA
ЮН	High-level output current	V _O = 5 V	125°C			1	μА
1225	Supply current	No load Outputs law	25°C		44	80	
DD	(four comparators)	No load, Outputs low	-55°C to 125°C			175	μА

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to VDD.

TLC3391 QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN N	XAM MC	UNIT
Supply voltage, V _{DD}	3	5 16	V
Common-mode input voltage, V _{IC}	-0.2	V _{DD} -1.5	V
Low-level : current, IOL		8 20	mA
Operating : ur temperature, TA	-40	85	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDIT	IONS†	MIN	TYP	MAX	UNIT	
		VIC = VICRMIN,	25°C		1.4	5		
۷io	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 4	-40°C to 85°C			7	mV	
	Input offset current	V _{IC} = 2.5 V	25°C	Tana	1		pΑ	
10	input onset current	VIC - 2.5 V	85°C			1	nA	
lum.	Input bias current	V _{IC} = 2.5 V	25°C		5		pA	
lВ	input bias current	VIC - 2.5 V	85°C			2	nA	
\/	Common-mode input voltage range		25°C	0 to V _{DD} -1			v	
VICR			-40°C to 85°C	0 to V _{DD} -1.5			V	
	Common-mode rejection ratio	emmon-mode rejection ratio V _{IC} = V _{ICR} min	25°C		84			
CMRR			85°C		84		dB	
			-40°C		84			
			25°C		85		dB	
KSVR	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	85°C		85			
		-40°C			84	-		
V	Law level autout voltage	$V_{ID} = -1 V$,	25°C		300	400	m\/	
VOL	Low-level output voltage	I _{OL} = 6 mA	85°C				m∨	
	High level output ourrent	V _{ID} = 1 V,	25°C		0.8	40	nA	
ЮН	High-level output current	V _O = 5 V	85°C			1	μА	
	Supply current	No lead Outputs law	25°C		44	80		
סס	(four comparators)	No load, Outputs low				125	μΑ	

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	3	5	16	V
Common-mode input voltage, VIC	-0.2		VDD-1.5	٧
Low-level output current, IOL		8	20	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITI	onst	MIN	TYP	MAX	TINU
		VIC = VICRMIN,	25°C		1.4	5	
VIO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 4	0°C to 70°C			6.5	mV
l	Input offset current	V _{IC} = 2.5 V	25°C		1		pΑ
10	input cliset current	VIC = 2.5 V	70°C		-	0.3	nA
li-	Input bias current	V _{IC} = 2.5 V	25°C		5		pA
ΙΒ	input bias current	VIC = 2.5 V	70°C			0.6	nA
V	Common-mode input voltage range		25°C	0 to Vpp-1			v
VICR			0°C to 70°C	0 to V _{DD} -1.5			•
~ * * * * * * * * * * * * * * * * * * *	Common-mode rejection ratio		25°C	127	84		dB
CMRR			70°C		84		
			0°C		84		
			25°C		85		dB
KSVR	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	70°C		85		
			0°C		85		
V-	Law level output voltage	$V_{ID} = -1 V$,	25°C		300	400	\/
VOL	Low-level output voltage	IOL = 6 mA	70°C			650	mV
10.00	Ulah laval autora averant	V _{ID} = 1 V,	25°C		0.8	40	nA
ЮН	High-level output current	put current VO = 5 V	70°C			1	μA
122	Supply current	No load. Outputs low	25°C	1	44	80	
ססי	(four comparators)	four comparators) No load, Outputs low	0°C to 70°C			100	μΑ

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

TLC339M, TLC339I, TLC339C QUADRUPLE MICROPOWER LincMOS™ COMPARATORS

switching characteristics, VDD = 5 V, TA = 25°C (see Figure 3)

	PARAMETER	TES	TEST CONDITIONS		MAX	UNIT	
			Overdrive = 2 mV	4.5			
		5000000	Overdrive = 5 mV	2.5			
	Propagation delay time, low-to-high level output	f = 10 kHz, C _I = 15 pF	Overdrive = 10 mV	1.7			
tPLH .	Propagation delay time, low-to-night level output	CL = 15 pr	Overdrive = 20 mV	1.2		μs	
			Overdrive = 40 mV	1.0			
		V _I = 1.4 V step at IN+ pin		1.1			
			Overdrive = 2 mV	3.6			
		4. (0.00)	Overdrive = 5 mV	2.1			
		f = 10 kHz,	Overdrive = 10 mV	1.3			
^t PHL	Propagation delay time, high-to-low level output	C _L = 15 pF	Overdrive = 20 mV	0.85		μs	
			Overdrive = 40 mV	0.55			
		V _J = 1.4 V ste	p at IN+ pin	0.10			
tтнL	Transition time, high-to-low level output	f = 10 kHz, C _L = 15 pF	Overdrive = 50 mV	20		ns	

PARAMETER MEASUREMENT INFORMATION

The TLC339 contains a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1 (a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1 (b) for the VICR test, rather than changing the input voltages, to provide greater accuracy.

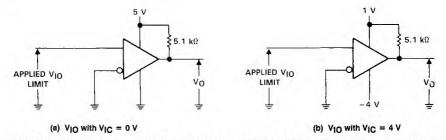


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output will change states.



PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

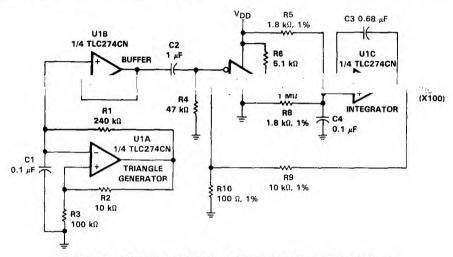
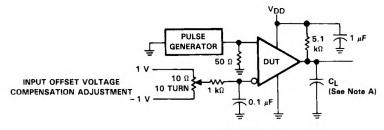


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

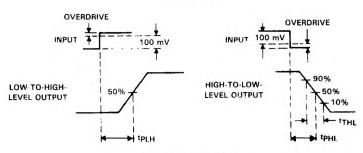
Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



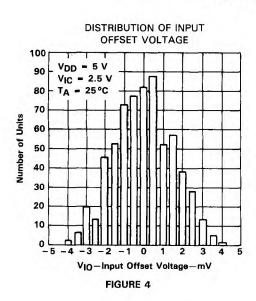
TEST CIRCUIT

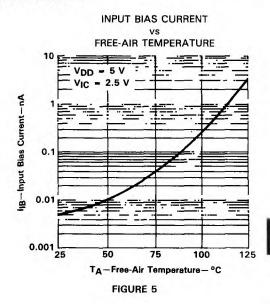


VOLTAGE WAVEFORMS

NOTE A: Ct includes probe and jig capacitance.

FIGURE 3. PROPAGATION DELAY, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS





POW-Women and the property of the property of

25 50 75

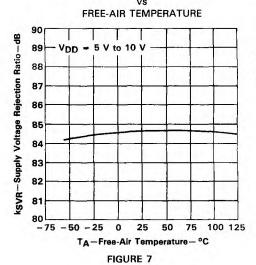
TA-Free-Air Temperature-°C

FIGURE 6

80

-75 -50 -25

COMMON-MODE REJECTION RATIO

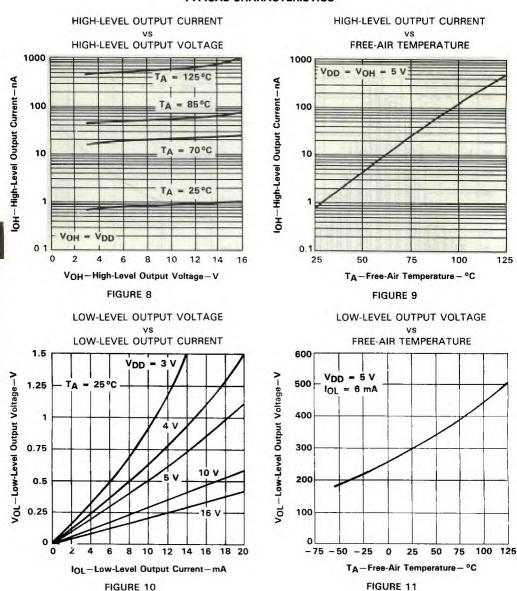


SUPPLY VOLTAGE REJECTION RATIO

100 125

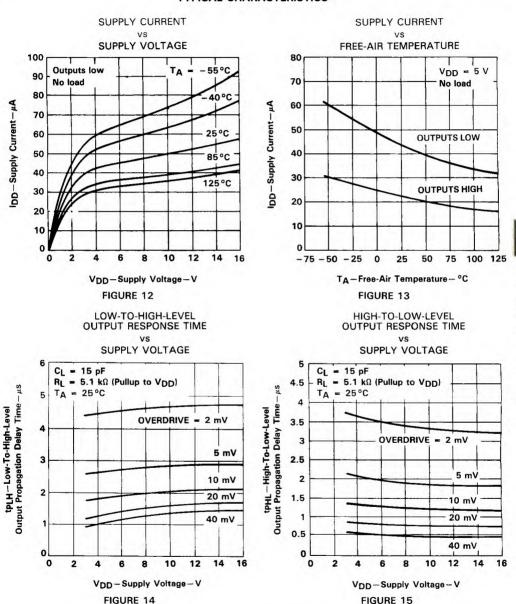


[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



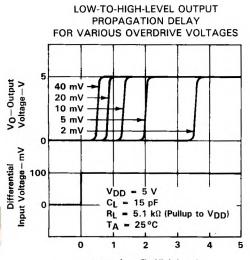
[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





tpLH-Low-To-High-Level Output Propagation Delay Time- μ s

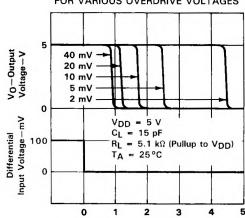
OUTPUT FALL TIME SUPPLY VOLTAGE 60 50 CL = 100 pF 40 t-Time-ns 50 pF 30 15 pF 20 10 $R_L = 5.1 \text{ k}\Omega \text{ (Pullup to VDD)}$ = 25°C TA 2 0 4 10 12 16 6 14 VDD-Supply Voltage-V

-DD c-pp., remage

FIGURE 16

FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES



tpHL—High-To-Low-Level Output Propagation Delay Time—μs

FIGURE 18



TLC339M, TLC339I, TLC339C OUADRUPLE MICROPOWER LincMOS™ COMPARATORS

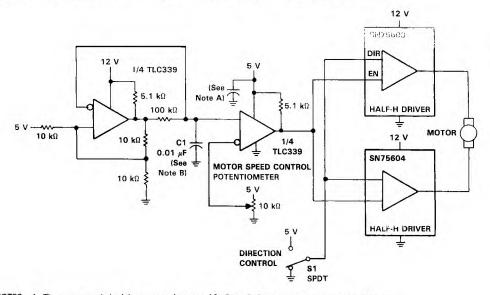
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with $V_{DD} = 5 \text{ V}$, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μ F) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC339 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

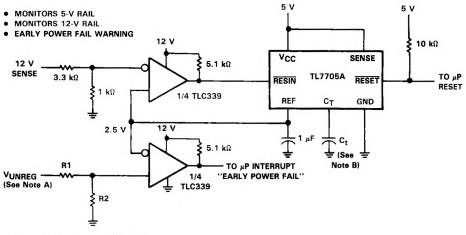


NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.

B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5 \left(\frac{R1 + R2}{R2} \right)$

B. The value of Ct determines the time delay of reset.

FIGURE 20. ENHANCED SUPPLY SUPERVISOR

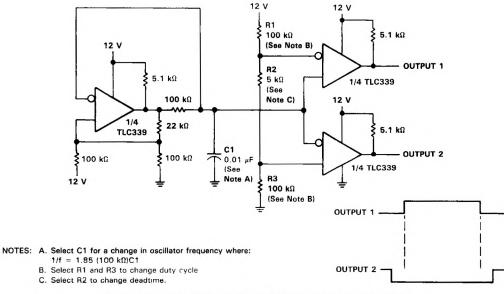


FIGURE 21. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TLC352M, TLC352I, TLC352C Lincmos™ Dual Differential Comparators

D2901 SEPTEMBER 1985-REVISED FEBRUARY 1989

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 1.4 V to 18 V
- Very Low Supply Current Drain 150 μA Typ at 5 V
 65 μA Typ at 1.4 V
- Built-In ESD Protection
- High Input Impedance . . . 1012 Ω Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM393

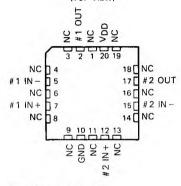
description

This device is fabricated LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than $10^{12} \Omega$), which allows direct interface to high-impedance sources. The outputs are nchannel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

TLC352M . . . JG PACKAGE
TLC352I, TLC352C . . . D, JG, OR P PACKAGE
(TOP VIEW)

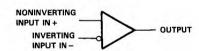


TLC352M . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

symbol (each comparator)



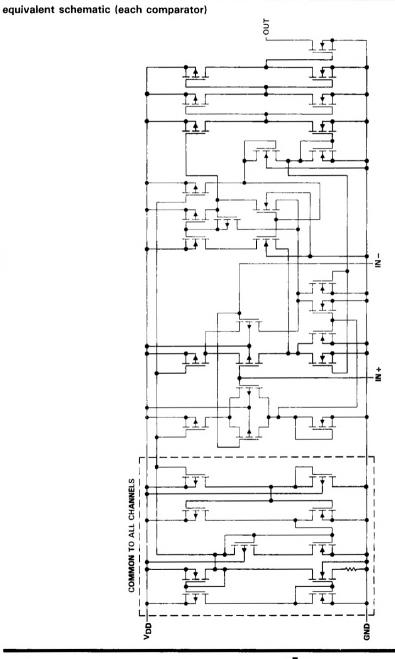
The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352M is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to $125\,^{\circ}$ C. The TLC352I is characterized for operation over the industrial temperature range of $-40\,^{\circ}$ C to $85\,^{\circ}$ C. The TLC352C is characterized for operation from $0\,^{\circ}$ C to $70\,^{\circ}$ C.

LinCMOS is a trademark of Texas Instruments Incorporated.









AVAILABLE OPTIONS

	V	PACKAGE					
TA	VIO MAX AT 25°C	SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)		
0°C to 70°C	5 mV	TLC352CD		TLC352CJG	TLC352CP		
-40°C to 85°C	5 mV	TLC352ID	=	TLC352IJG	TLC352IP		
-55°C to 125°C	5 mV		TLC352MFK	TLC352MJG	-		

D packages are availabe taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC352CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)	18 V
Differential input voltage, VID (see Note 2)	. ±18 V
Input voltage, V _I	
Input voltage range	V to 18 V
Output voltage, Vo	18 V
Input current, I	. ±5 mA
Output current, Io	. 20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation	ting Table
Operating free-air temperature range: TLC352M	to 125°C
TLC352I40°	C to 85°C
TLC352C 0°4	C to 70°C
Storage temperature range65°C	to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.

- 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
- 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	TA ≤ 25°C PO∴! II RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWLH RATING	TA = 125°C POWER RATING
D	nW	5.8 mW/°C	64°C	464 mW	nW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG (TLC352M)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (TLC352I, TLC352C)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A



recommended operating conditions

		M SUFFIX	×	US-I	I-SUFFIX	0	C-SUFFIX		LINE
		MIN "ICM MAX MIN NOM MAX MIN NOM MAX	MAX	MIN	OM MAX	Z	NOM	MAX	
Supply voltage, VDD		4	16	က	16	8		16	>
	V _{DD} = 5 V	0	3.5	0	3.5	0		3.5	;
Common-mode input voitage, VIC	V _{DD} = 10 V	0	8.5	0	8.5	0		8.5	>
T entitorement six sent parities		r r	125	-40	85	C		70	Jo 02

electrical characteristics at specified free-air temperature, VDD = 1.4 V (unless otherwise noted)

1	Secretary of the second		*			TLC352M			TLC3521		Ť			!
≥ 2	PARAMETER	TEST	TEST CONDITIONS		NIN	TYP	MAX	MIN	TYP	MAX	NIE	-11-	MAX	
1 2				25°C		2	2		2	2		2	5	- N
=	VIO Input offset voltage	VIC = VICR min, see Note 4	See Note 4	Full range			10			7			6.5	A
				25°C		-			-			1		ρA
_	Input offset current			MAX TA			10			1			0.3	ηA
				25°€		æ			2			2		ρĄ
_	Input bias current			MAX TA			20			2			9.0	n.A
1.75	Common-mode input				0 to			0 to			0 to			>
9	VICR voltage range			Luc range	0 2			0.2			0.2			>
l o	Low-fevel			25°C		100	200		100	200		100	200	Man
2	output voltage	VID = -0.5 V.	10L = 0.6 mA	Full range			200			200			200	2
Ų.	Low-level	V = 0 = 0.5V	Vo. = 0.3 V	25°C	-	1.6		-	9.		-	9,		ĄE
51	output current	- 1	70.						5	b				
	Supply current	X 9 0X	To CIV	25°C		65	150		65	150		65	150	4.
2	(two comparators)	VDD = 0.3 V.	0.00	Full range			200			200			200	1

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC352M, 0°C to 70°C for TLC352C, and -40°C to 85 °C for TLC3521. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD} They

can be verified by applying the limit value to the input and checking for the appropriate output state.

Voltage Comparators

3

LIND >E Ad Ą Ad Αu Y. >= 4 A Ψ > Ą 6.5 0.3 9.0 9 700 0.3 TLC352C TYP ın 0.1 50 0 15 VpD-15 Vpp-1 o to 0 to 0 MAX 400 8 0.3 0.4 TLC3521 TYP 0.1 9 0.15 20 Vop-1 Vpp-15 0 to 0 10 NIN MAX 9 9 20 400 90 0.3 4.0 TLC352M TYP 0.1 0.15 150 16 V_{DD}-1.5 VDD-1 0 to 0 to ME 9 MAX TA MAX TA Full range Full range Full range Full range Full range 25°C 25°C 25°C 25 °C 25°C 25 °C 25 °C 25°C VOH = 15 V = 1.5 V = 5 \ = 4 mA TEST CONDITIONS See Note No load VOH Vol P_C = VICR min, · 1 < = -1 V. VDD = 1 V. = 1 \ QI ۵N VIC. Q, Common-mode input Input offset voltage Input offset current (two comparators) Input bias current output voltage Supply current PARAMETER output current output current voltage range High-level Low-level Low-level VICR N_{IO} VOL HO aa 9 8 10

electrical characteristics at specified free-air temperature, VDD = 5 V (unless otherwise noted)

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC352M, 0°C to 70°C for TLC352C, and -40°C The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-81 resistor between the output and V_{DD}. They to 85 °C for TLC3521. IMPORTANT. See Parameter Measurement Information.

can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, VDD = 5 V, TA = 25 °C

PARAMETER	TEST CONDITIONS	VDITIONS	MIN	MIN TYP MAX UN	MAX	ร์
	RL connected to 5 V through 5.1 kΩ,	RL connected to 5 V through 5.1 kg, 100-mV input step with 5-mV overdrive		029		•
uespouse nue	C _L = 15 pF [‡] , See Note 5	TTL-level input step		200		

Ę

[‡]C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

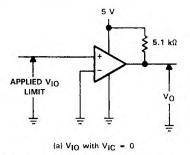
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.



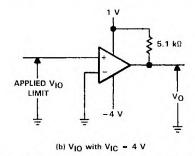


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS



Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

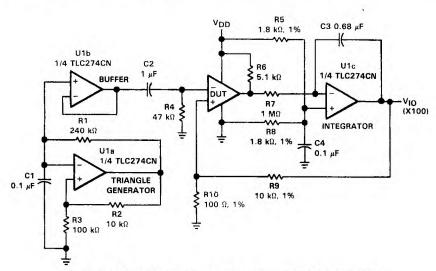
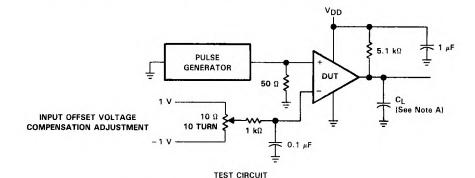
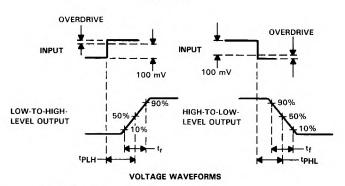


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.





NOTE A: CL includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS



TLC354M, TLC354I, TLC354C Lincmos™ Quadruple Differential Comparators

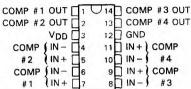
D2901, SEPTEMBER 1985-REVISED FEBRUARY 1989

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 1.4 V to 18 V
- Very Low Supply Current Drain 300 μA Typ at 5 V
 130 μA Typ at 1.4 V
- Built-In ESD Protection
- High Input Impedance . . . 1012 Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM339

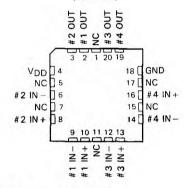
description

This device is fabricated LinCMOS™ technology and consists of four independent voltage comparators; each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 1012 Ω), which allows direct interface to high-impedance sources. The outputs are nchannel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC354 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

TLC354M . . . J PACKAGE TLC354I, TLC354C . . . D OR N PACKAGE (TOP VIEW)

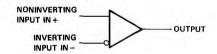


TLC354M . . . FK PACKAGE



NC-No internal connection

symbol (each comparator)



The TLC354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC354M is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The TLC354I is characterized for operation over the industrial temperature range of $-40\,^{\circ}$ C to 85 $^{\circ}$ C. The TLC354C is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

LinCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator) OUT ż COMMON TO ALL CHANNELS



TLC354M, TLC354I, TLC354C LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

AVAILABLE OPTIONS

	V . MAY		PACE A	GE	
TA	VIO MAX AT 25°C	SMALL-OUTLINE (D)	CHIP CARRILK (FK)	CERAMIC DIP	PLASTIC DIP
0°C to 70°C	5 mV	TLC354CD	_	TLC354CJ	TLC354CN
-40°C to 85°C	5 mV	TLC354ID		TLC354IJ	TLC354IN
-55°C to 125°C	5 mV	-	TLC354MFK	TLC354MJ	-

D packages are availabe taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC354CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)
Differential input voltage, VID (see Note 2)
Input voltage, VI
Input voltage range0.3 V to 18 V
Output voltage, Vo
Input current, I) ±5 mA
Output current, IO
Duration of output short-circuit to ground (see Note 3) unlimited
Continuous total dissipation See Dissipation Rating Table
Continuous total dissipation
그 마을 마음이 살아왔다면 하는 이렇게 하는 아이들이 살아들이 살아 있다. 이 사람들은 아이들이 아이들은 아이들은 아이들은 아이들은 아이들은 아이들은 아이
Operating free-air temperature range: TLC354M
Operating free-air temperature range: TLC354M
Operating free-air temperature range: TLC354M -55°C to 125°C TLC354I -40°C to 85°C TLC354C 0°C to 70°C
Operating free-air temperature range: TLC354M -55°C to 125°C TLC354I -40°C to 85°C TLC354C 0°C to 70°C Storage temperature range -65°C to 150°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.

- 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
- 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	494 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC354M)	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC354I, TLC354C)	500 mW	N/A	N/A	500 mW	500 mW	N/A
N	500 mW	N/A	N/A	500 mW	500 mW	N/A

Voltage Comparators

recommended operating conditions

		M-SUFFIX	FFIX	-	X) : Ii : -		Ċ	C-SUFFIX		TIMIT
		MIN NOM	M MAX	MIN		MAX	MIN	MIN THE MAX MIN NOM MAX	MAX	
Supply voltage, VDD		1.4	16	1.4		16	1.4		16	>
4	V _{DD} = 5 V	0	3.5	0		3.5	0		3.5	>
Common-mode input voitage, vic	$V_{DD} = 10 V$	0	8.5	0		8.5	0		8.5	
Operating free-air temperature, TA		- 55	125	- 40		82	0		70	ာ့

electrical characteristics at specified free-air temperature, VDD = 1.4 V (unless otherwise noted)

	-	1011	Township Town			TLC354M	5		TI:41			TLC354C		TIMIT
	PAKAMEIEK		CONDITIONS		NIW	TYP	MAX	MIN	116	MAX	MIN	TYP	MAX	
				25°C		2	5		2	5		2	5	7
0	VIO Input offset voitage	VIC = VICR min, see Note 4	See Note 4	Full range			10			7			6.5	È
				25°C		-			-			-		ΡA
<u>o</u>	Input offset current			Α_			10			1			0.3	ν
						5			2			2		ρĄ
8	Input bias current			MAX TA			20			2			9.0	Α'n
19	Common-mode input			25.00	0 10			0 to			0 to			>
VICR.	voltage range			2 23	0.2			0.2			0.2			
	High-level	7	VOH = 5 V	25°C		0.1			0.1			0.1		νV
Ę.	output current	A = QIA	V _{OH} = 15 V	Full range			1			1			1	μА
	Low-level	3		25°C		100	200		100	200		100	200	1
VO.	output voltage	V1D = -0.5 V, 10L = 0.8 mA	OF = 0.0 mA	Futl range			200			200			200	A L
	Low-level	V = 0 V	V= 300 =- V	J. 36		9		,	4			4		É
ק	output current	'A 6:0 - Ola	*OL - 300 IIIV			2			2		-			
	Supply current	N = 0 = N	No lead	25°C		130	300		130	300		130	300	•
9	(four comparators)	, c.o = 00a	No load	Full range			400			400			400	¥.

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC354M, -40°C to 85°C for TLC354M, and 0°C NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kD resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state. to 70°C for TLC354C. IMPORTANT See Parameter Measurement Information.

IN SI

LINO È Ā 4 M A A > Ā F 9.0 MAX 9 12 0.3 400 700 TLC354C TYP 150 0.1 VDD-15 Vpp-1 0 10 Z MAX 0 13 2 400 200 TLC3541 TYP 0.1 150 VDD-15 Vnn-1 000 0 0 Z MAX 10 12 10 20 400 200 : 2 2 150 0.1 VDD - 15 Vpp-1 0 to O to MES Full range MAX TA Full range Full range MAX TA Full range 25°C 25°C 25°C 25°C 25°C 25°C VOH = 15 V 101 = 4 mA $V_{OH} = 5 V$ TEST CONDITIONS See Note 4 = VICR min. = -1 V, 1 < VIC. 2 < ۵i/ Common-mode input Input offset voltage Input offset current Input bias current PARAMETER output current output voitage voltage range High-level Low-level VICR 2 VOL 9 F 9

5 V (unless otherwise noted)

electrical characteristics at specified free-air temperature, VDD =

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC354M. -40°C to 85°C for TLC354I, and 0°C to 70°C for TLC354C IMPORTANT. See Parameter Measurement Information.

E 4

16

9

16

9

16

9

25°C

= 1.5 V

-1 V.

ú

Supply current

Low-level

9.0

0.8

8.0

Full range

Vol =

VDD = 1 V.

(four comparators)

90

03

9.0

0.3

VOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kD resistor between the output and VDp. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, VDD = 5 V, $TA = 25 ^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	ADITIONS	MIN	TYP MAX U	MAX	2
omit connection	RL connected to 5 V through 5.1 kΩ,	RL connected to 5 V through 5.1 kg, 100-mV input step with 5-mV overdrive		650		
nesponse mine	C _L = 15 pF [‡] , See Note 5	TTL-level input step		200		

[‡]CL includes probe and jig capacitance

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V

The digital output stage of the TLC354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the VICR test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

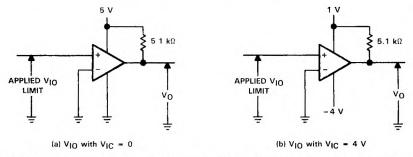


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

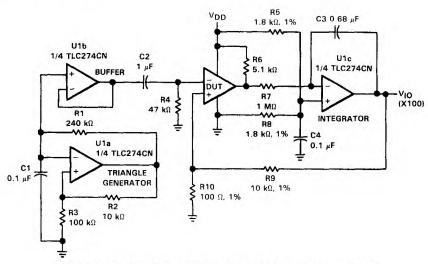
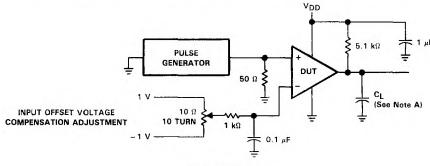
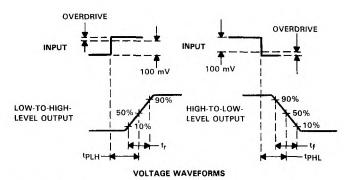


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



NOTE A: CL includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

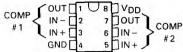
- Wide Range of Supply Voltages . . . 2 V to 18 V
- Very Low Supply Current Drain 150 μA
 Typ at 5 V
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 1012 Ω Tvp
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM393

description

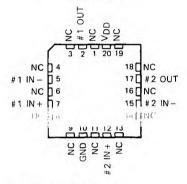
And they

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 V. Each device features extremely high input impedance (typically greater than 1012 Ω) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

TLC372M . . . JG PACKAGE
TLC372I, TLC372C . . . D, JG, OR P PACKAGE
(TOP VIEW)

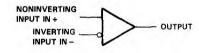


TLC372M . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

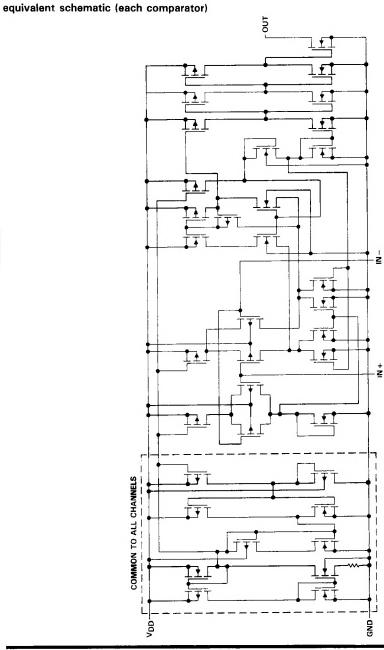
symbol (each comparator)



The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to $125\,^{\circ}$ C. The TLC372I is characterized for operation from $-40\,^{\circ}$ C to $85\,^{\circ}$ C. The TLC372C is characterized for operation from $0\,^{\circ}$ C to $70\,^{\circ}$ C.

LinCMOS is a trademark of Texas Instruments Incorporated.





TLC372M, TLC372I, TLC372C LinCMOS™ DUAL DIFFERENTIAL COMPARATORS

AVAILABLE OPTIONS

	V NAV		PACKA	GE	
TA	VIO MAX AT 25°C	SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP
o°C to 70°C	5 mV	TLC372CD	-	TLC372CJG	TLC372CP
-40°C to 85°C	5 mV	TLC372ID	-	TLC372iJG	TLC372IP
-55°C to 125°C	5 mV	-	TLC372MFK	TLC372MJG	-

D packages are availabe taped and reeled. Add "R" suffix to device type (e.g., TLC372CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)	18 V
Differential input voltage, VID (see Note 2)	± 18 V
Input voltage, VI	
Output voltage, Vo	
Input current, II	
Output current, In	
Duration of output short-circuit to ground (see Note 3)	
Continuous total dissipation See	
Operating free-air temperature range: TLC372M	^ - [- [- [- [- [- [- [- [- [-
TLC372I	
TLC372C	
Storage temperature range	
Case temperature for 60 seconds: FK package	
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds. D or P package	
Load temperature 1,0 mm (1,10 mem, nom case for 10 seconds, b of 1 packet	.gc 200 C

- NOTES: 1. All voltage values except differential voltages are with respect to network ground.
 - 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
 - 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG (TLC372M)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (TLC372I, TLC372C)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A

Voltage Comparators

recommended operating conditions

		N. JIFFIX	×	IS-I	-SUFFIX		C-SUFFIX	×	FIMIL
		MIN W MAX MIN NOM MAX, MIN NOM MAX	MAX	MIN	NOM MA	× ×	NON NI	MAX	
Supply voltage, VDD		4	16	3		١.	3	16	>
	VDD = 5 V	0	3.5	0	3	3.5	0	3.5	>
Common-mode input voitage, VIC	V _{DD} = 10 V	0	8.5	0	8	8.5	0	8.5	>
Operating free-air temperature, TA		-55	125	125 -40		85	0	70	၁

electrical characteristics at specified free-air temperature, VDD = 5 V (unless otherwise noted)

TLC372C	TYP MAX	1 5	6.5	1 pA	0.3 nA	5 pA	0.6 nA		^			0.1 nA	1 µA	150 400	700	16		150 300	
TLC	MIN							0 to	VDD-1	0 to	VpD-15					ď	,		
	MAX	5	7		1		2						1	400	700			300	
TLC372I	MIN TYP	-		L.		5		0 to	Vop -1	0 to	V _{DD} - 1.5	0.1		150		4		150	
	MAX	2	10		10		20		,		N.		3	400	700			300	
≥ .	MIN F	-		-		9		0 to	Vpp-1	0 to	V _{DD} - 1.5	0.1		150		4		150	
		25°C	Full range	26.00	TA	,,	MAX TA	25°C		Endl report	-	25°C	Ful i :e		Full range	25.05	2 22	25°C	
tomorphism to	CONDITIONS	•	See Note 4									VOH = 5 V	VOH = 15 V		10L = 4 mA	Ve. = 1 E V	*OL = 10 *		
-	2		VIC = VICR MIN,									7.	A 1 = QIA		VID = -1 V,	V 1 V	'A - GIA		
	PAKAMETEH		V _I O Input offset voitage		Input offset current		Input bias current		Common-mode input	voltage range		High-level	output current	Low-level	output voltage	Low-level	output current	Supply current	
		5	0		0		<u>8</u>			VIC.B			НОН		VOL.		.0F		

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C, and -40°C to 85 °C for TLC372I. IMPORTANT: See Parameter Measurement Information.

NOTE 2: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kit resistor between the output and Vpp. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, VDD = 5 V, TA = 25 °C

PARAMETER	TEST CO	TEST CONDITIONS	Z	MIN TYP MAX UNIT	TINO
	R _L connected to 5 V through 5.1 kΩ,	RL connected to 5 V through 5.1 kg, 100-mV input step with 5-mV overdrive		650	-
Hesponse mine	C _I = 15 pF [‡] , See Note 5	TTL-level input step		200	€

[‡] C<u>L</u> includes probe and jig capacitance. NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



The digital output stage of the TLC372 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

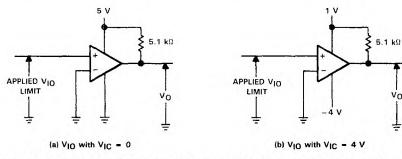


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

Figure 2 illustrates a practical circuit for direct do measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

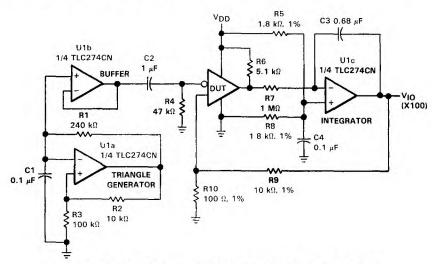
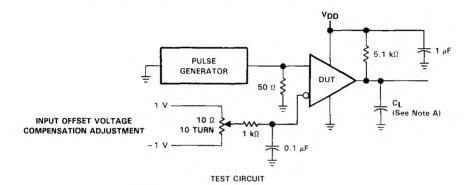
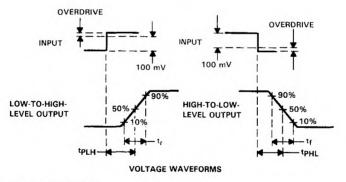


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.





NOTE A: CL includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TLC374M, TLC374I, TLC374C Lincmos™ Quadruple Differential Comparators

D2783, NOVEMBER 1983-REVISED SEPTEMBER 1988

- Single or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 2 V to 18 V
- Very Low Supply Current Drain 0.3 mA Typ at 5 V
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 1012 Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM339

description

This device fabricated is using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 V. Each device features extremely high input impedance (typically greater than $10^{12} \Omega$) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under

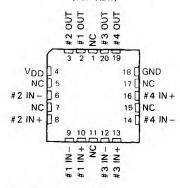
MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The TLC374I is characterized for operation from $-40\,^{\circ}$ C to 85 $^{\circ}$ C. The TLC374C is characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

TLC374I, TLC374C . . . D, J, OR N PACKAGE (TOP VIEW) COMP #1 OUT 1 U14 COMP #3 OUT COMP #2 OUT 13 COMP #4 OUT VDD [3 12 GND COMP (IN-11 | IN+ COMP #2 IN+ 15 10 N - 1 #4 COMP IN- [9 | IN+ COMP 8 | IN- #3 IN+ #1

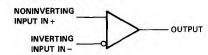
TLC374M . . . J PACKAGE

TLC374M . . . FK PACKAGE (TOP VIEW)



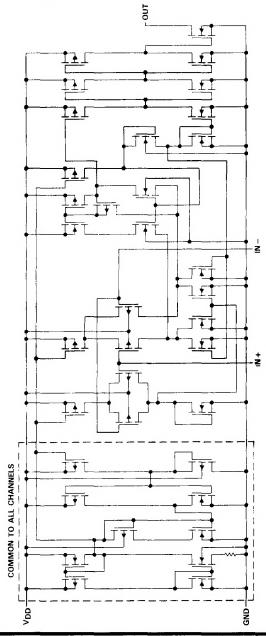
NC-No internal connection

symbol (each comparator)



LinCMOS is a trademark of Texas Instruments Incorporated.





TLC374M, TLC374I, TLC374C LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

AVAILABLE OPTIONS

	V		PACKA	GE	
TA	VIO MAX AT 25°C	SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP
0°C to 70°C	5 mV	TLC374CD	-	TLC374CJ	TLC374CN
-40°C to 85°C	5 mV	TLC374ID	-	TLC374IJ	TLC374IN
-55°C to 125°C	5 mV	=	TLC374MFK	TLC374MJ	-

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TLC374CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)		V
Differential input voltage, VID (see N	ote 2) ±18 \	V
	V _{DI}	
Input voltage range	0.3 V to 18 V	٧
Output voltage, Vo		V
Input current, IJ	±5 m/	A
Output current, IO		Α
Duration of output short-circuit to gro	ound (see Note 3) unlimite	d
Continuous total dissipation	See Dissipation Rating Table	е
: " (1885년 - 1885년 - 1845년 - 1885년 - 1		
: " (1885년 - 1885년 - 1845년 - 1885년 - 1	그런 이 나는 아이들은 그렇게 하는 것은 것이 없는데, 이 이렇게 되었다고 있다면 하는데 그렇게 하는데 그렇게 되었다면 하는데 얼마를 하는데 없다고 있다고 있다면 하는데 없었다.	С
: " (1885년 - 1885년 - 1845년 - 1885년 - 1	TLC374M55°C to 125°C	C
Operating free-air temperature range:	TLC374M55 °C to 125 °C TLC374I40 °C to 85 °C	CCC
Operating free-air temperature range: Storage temperature range	TLC374M55 °C to 125 °C TLC374I40 °C to 85 °C TLC374C 0 °C to 70 °C	CCCC
Operating free-air temperature range: Storage temperature range Case temperature for 60 seconds: Fi	TLC374M -55 °C to 125 °C TLC374I -40 °C to 85 °C TLC374C 0 °C to 70 °C -65 °C to 150 °C	00000

NOTES: 1. All voltage values except differential voltages are with respect to network ground.

- 2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
- 3. Short circuits from outputs to VDD can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE TA	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	500 mW	7.6 mW/°C	84°C	494 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC374M)	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC374I, TLC374C)	500 mW	N/A	N/A	500 mW	500 mW	N/A
N	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		N-S	M-SUFFIX	i	FSILE FIX		ڼ	C-SUFFIX	F	FIMIL
		MIN	MIN NOM MAX MIN N:M MAX MIN NOM MAX	Z	2	MAX	MIN	NOW	MAX	5
Supply voltage, VDD		4	16	3		16	3		16	>
	V _{DD} = 5 V	0	3.5	0		3.5	0		3.5	;
Common-mode input voitage, VIC	$V_{DD} = 10 V$	0	8.5	0		8.5	0		8.5	>
Operating free-air temperature, TA		- 55	125	125 -40		85	0		70	၁့

electrical characteristics at specified free-air temperature, VDD = 5 V (unless otherwise noted)

						TLC374M	-	TLC3741	741		110	1LC3/4C	Ī	-
	PARAMETER	TES	TEST CONDITIONS		5	ТУР	MAX	MIN TYP		MAX	MIN	TYP	MAX	ONI
				25°C	L	1	2		1	2		-	ıcı	1
0/	Input offset voltage	VIC = VICR min,	See Note 4	Full range			01			7			6.5	2
1				25°C		-			1			1		bA
	Input offset current			MAX TA			10			-			0.3	νV
1				25°C	Ì	S.			5			2		ρĄ
	Input bias current			MAX TA			20			2			9.0	ν
1	Common-mode input			25°C	0 to Vnn - 1	-		0 to Vpp - 1			0 to V _{DD} = 1		8-1	
	VICR voltage range			Full range	0 to			0 to			0 to			>
			A Comment of the last of the l		Vpp-1.5	1.5		Vpg-15			VDD-15			
1	High-level		VOH = 5 V	25°C		0.1		0 1	1			0.1		ν
	output current	V1 = 01V	VOH = 15 V	Full range			-			-			1	Pη
1	Low-fevel			25°C		150 4	400	150		400		150	400	1
VOL	output voltage	VID = -1 V,	OL = 4 mA	Full range		7	200		7	200			200	È
	Low-level output current	V _{ID} = -1 V,	VOL = 15 V	25°C	φ	16		9	16		9	91		Αm
1	Supply current			25°C		300	009	300		009		300	900	
	(four comparators)	VID = 1 V,	No load	Full range		80	800		8	800			800	Į.

All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C for TLC374M, 0°C to 70°C to 85°C for TLC3741. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-k0 resistor between the output and VDD. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, VDD = 5 V, TA = 25 °C

PARAMETER	TEST COND-11-)N(SN(-11-	Z	TYP	TYP MAX UNI	5
	RL connected to 5 V through 5.1 kB,	mV input step with 5-mV overdrive		650		
Hesponse nue	C _I = 15 pF [‡] , See Note 5	TTL-level input step		200		2

‡C_L includes probe and jig capacitance. NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



TLC374M, TLC374I, TLC374C LinCMOS™ QUADRUPLE DIFFERENTIAL COMPARATORS

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC374 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

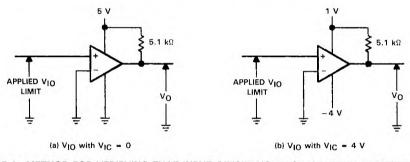


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

Voltage Comparators

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

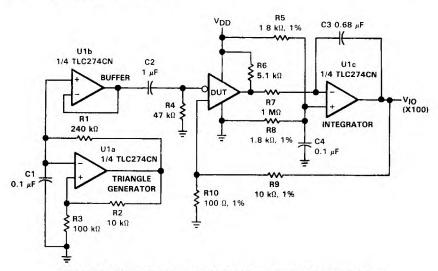
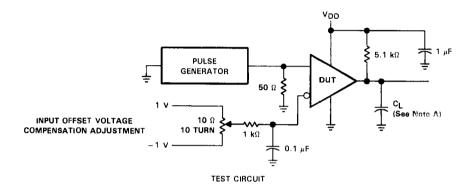
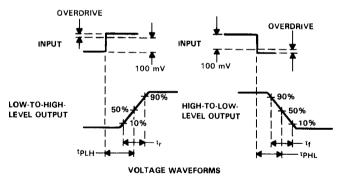


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.





NOTE A: CL includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

• Single Supply Operation:

TLC393M . . . 4 V to 16 V TLC393I . . . 3 V to 16 V TLC393C . . . 3 V to 16 V

- High Input Impedance . . . 1012 Ω Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

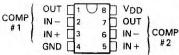
description

The TLC393 consists of two independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3702 data sheet.

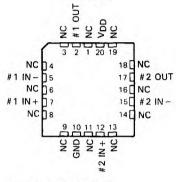
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393M is characterized for operation over the full military temperature range of $-55\,^{\circ}\text{C}$ to 125 °C. The TLC393I is characterized for operation over the extended industrial temperature range of $-40\,^{\circ}\text{C}$ to 85 °C. The TLC393C is characterized for operation over the commercial temperature range of 0 °C to 70 °C.

TLC393M . . . JG PACKAGE
TLC393I, TLC393C . . . D, JG, OR P PACKAGE
(TOP VIEW)

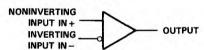


TLC393M . . . FK PACKAGE



NC-No internal connection

symbol (each comparator)



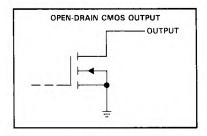
AVAILABLE OPTIONS

			PAC	KAGE	
TA	V _{IO} max at 25°C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC393CD	-	TLC393CJG	TLC393CF
-40°C to 85°C	5 mV	TLC393ID	-	TLC393IJG	TLC393IP
-55°C to 125°C	5 mV		TLC393MFK	тьсз93млс	i ell

The D package is available taped and reeled. Add the suffix R to the device type. (e.g., TLC393CDR)

LinCMOS is a trademark of Texas Instruments Incorporated.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)
Differential input voltage (see Note 2) ±18 V
Input voltage, V 0.3 V to V _{DD}
Output voltage, VO
Input current, I
Output current, IO (each output)
Total supply current into V _{DD} terminal
Total current out of ground terminal
Continuous total dissipation See Dissipation Rating Table
Operating free-air temperature range: TLC393M
TLC393I40°C to 85°C
TLC393C 0°C to 70°C
Storage temperature range65°C to 150°C
Case temperature for 60 seconds: FK package
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package 300 °C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	= "
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (TLC393M)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	528 mW	429 mW	4 - A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	-



TLC393M DUAL MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	4	5	16	٧
Common-mode input voltage, V _{IC}	0		V _{DD} - 1.5	٧
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	-65		125	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDI	TIONS [†]	MIN	TYP	MAX	UNIT
		V _{IC} = V _{ICR} min,	25°C		1.4	5	
VIO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	-55°C to 125°C			10	mV
li =	Input offset current	V _{IC} = 2.5 V	25°C		1		pA
lo lo	input offset current	VIC = 2.5 V	125°C			15	nΑ
lin	Input bias current	V _{IC} = 2.5 V	25°C		5		pA
IB	input bias current	VIC = 2.5 V	125°C			30	nA
			25°C	0 to			
V	Common mode input voltage commo		25-0	V _{DD} - 1			V
VICR	CR Common-mode input voltage range		-55°C to 125°C	0 to V _{DD} - 1.5			V
			25°C		84		
CMRR	Common-mode rejection ratio	Common-mode rejection ratio V _{IC} = V _{ICR} min	125°C		84		dB
			-55°C		84		
			25 °C		85		
KSVR	Supply voltage rejection ratio	$V_{DD} = 5 V \text{ to } 10 V$	125°C		84		dB
			-55°C		84		
Va.	Low-level output voltage	$V_{ID} = -1 V$,	25°C		300	400	
VOL	Low-lever output vortage	IOL = 6 mA	125°C			800	m∨
1	High-level output current	$V_{ID} = 1 V$	25°C		0.8	40	nA
ЮН	riigir-ievei output current	$V_0 = 5 V$	125°C			1	μΑ
(m.m.	Sundy surrent (both surrent)	No load,	25°C		22	40	
IDD	Supply current (both comparators)	Outputs low	-55°C to 125°C			90	μΑ

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

PARAMETER

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	3	5	16	٧
Common-mode input voltage, VIC	-0.2	1	V _{DD} − 1.5	٧
Low-level output current, IQL			20	mA
Operating free-air temperature, TA	-40		85	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

MAX UNIT

	PARAMETER	IESI CUNDI	IION9.	IAIIIA	III	MINY	Olati	
VIO	Input offset voltage	V _{IC} = V _{ICR} min, 25 °C		Ī	1.4	5		
		V _{DD} = 5 V to 10 V, See Note 4	-40°C to 85°C			7	mV	
	Company Community of the Community of th	V 25V	25°C		1		pΑ	
Ю	Input offset current	V _{IC} = 2.5 V	85°C			1	nA	
¹IB	Input bias current	V _{IC} = 2.5 V	25°C		5		pΑ	
			85 °C			2	nA	
VICR	Common-mode input voltage range	,	25°C	0 to V _{DD} – 1			V	
			-40°C to 85°C	0 to V _{DD} – 1.5			V	
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min	25 °C		84			
			85°C		84		dB	
			-40°C		84			
ksvr	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	25°C		85			
			85°C		85		dB	
			-40°C		84			
VOL	Low-level output voltage	$V_{ID} = -1 V$	25 °C			400	mV	
		IOL = 6 mA	85°C			700	mv	
7 11		V _{ID} = 1 V,	25°C		8.0	40	nA	
ЮН	High-level output current	V ₀ = 5 V	85°C			1	μΑ	
IDD	Supply current (both comparators)	No load,	25°C		22	40		
		Outputs low	-40°C to 85°C			65	μА	

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted. NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3	5	16	V
Common-mode input voltage, V _{IC}	-0.2		V _{DD} - 1.5	٧
Low-level output current, IOL		4	20	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]		MIN	TYP	MAX	UNIT	
V _{IO}	Input offset voltage	V _{IC} = V _{ICR} min,	25 °C		1.4	5		
		$V_{DD} = 5 V \text{ to } 10 V$, See Note 4	0°C to 70°C			6.5	mV	
110	Input offset current	V _{IC} = 2.5 V	25 °C		1		pA	
			70°C			0.3	nΑ	
IB	Input bias current	V _{IC} = 2.5 V	25 °C		5		pΑ	
			70°C			0.6	nA	
VICR	Common-mode input voltage range		25 °C	0 to V _{DD} – 1				
			0°C to 70°C	0 to V _{DD} - 1.5			V	
	Common-mode rejection ratio	V _{IC} = V _{ICR} min	25 °C		84			
CMRR			70°C		84		dB	
			0°C		84			
	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	25°C		85			
ksvr			70°C		85		dB	
			0°C		85			
	Low-level output voltage	$V_{ID} = -1 V$,	25°C		300	400	mV	
VOL		IOL = 6 mA	70°C			650		
юн	High-level output current	V _{ID} = 1 V,	25°C		0.8	40	nA	
		$V_0 = 5 V$	70°C			1	μΑ	
IDD	Supply current (both comparators)	No load,	25 °C		22	40	_	
		Outputs low	0°C to 70°C			50	μΑ	

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

TLC393M, TLC393I, TLC393C DUAL MICROPOWER LinCMOS™ COMPARATORS

switching characteristics, VDD = 5 V, TA = 25°C (see Figure 3)

PARAMETER		TEST	TEST CONDITIONS		MAX	UNIT	
	Propagation delay time, low-to-high level output		Overdrive = 2 mV	4.1	5	T	
		f = 10 kHz, C _L = 15 pF	Overdrive = 5 mV	2.1	5	İ	
			Overdrive = 10 mV	1.3	7	μs	
tPLH Propagation			Overdrive = 20 mV	1.:	2		
			Overdrive = 40 mV	1.			
		V _I = 1.4 V step at IN+ pin		1.		1	
	Propagation delay time, high-to-low level output		Overdrive = 2 mV	3.0	3	μs	
		f = 10 kHz, C _L = 15 pF Overdrive = 5 mV 2.1 Overdrive = 10 mV 1.3 Overdrive = 20 mV 0.85 Overdrive = 40 mV 0.55	Overdrive = 5 mV	2.			
			Overdrive = 10 mV	1.:	3		
tpHL Propagation			Overdrive = 20 mV	0.8	5		
			5				
		V _I = 1.4 V step at IN+ pin		0.10)		
	Transition time, high-to-low level output	f = 10 kHz,	Outsideline 50 mV	20			
t _{THL} Transition tir		C _L = 15 pF	Overdrive = 50 mV	20	,	ns	



The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

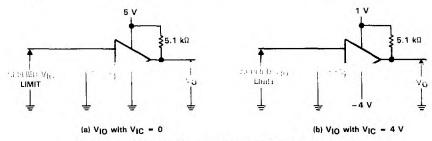


FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo-loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

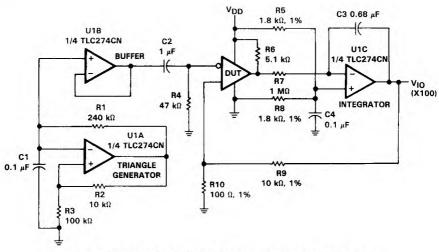
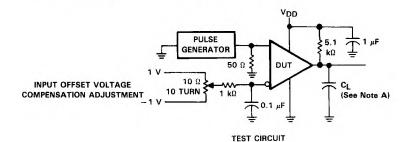
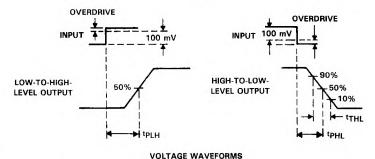


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.

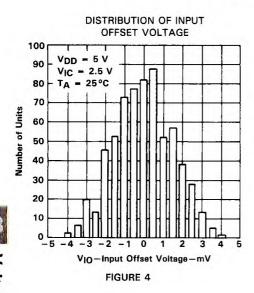


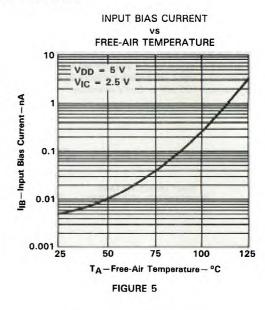


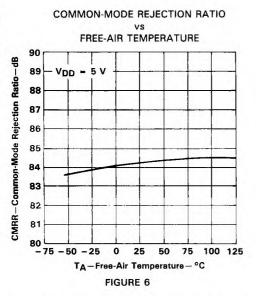
NOTE A: CL includes probe and jig capacitance.

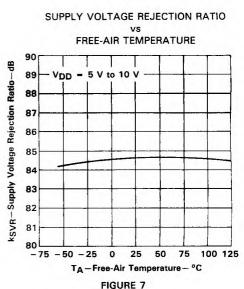
FIGURE 3. PROPAGATION DELAY, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS[†]





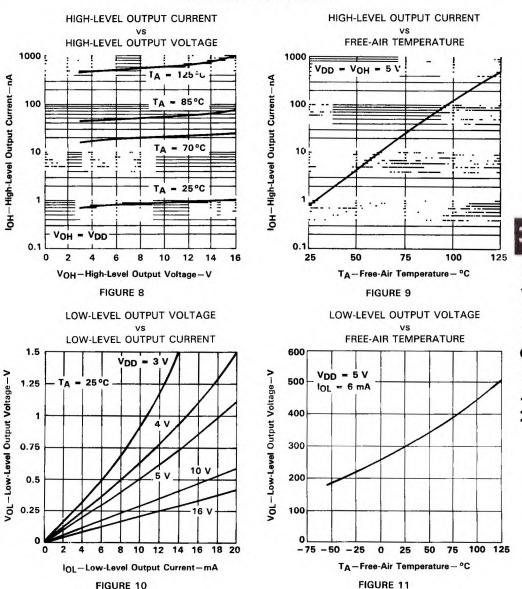




Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices



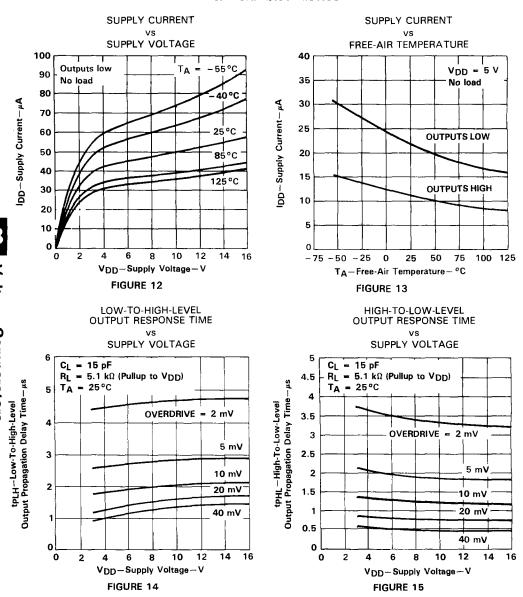
TYPICAL CHARACTERISTICS†



[†]Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



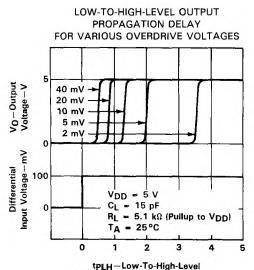
TYPICAL CHARACTERISTICS[†]

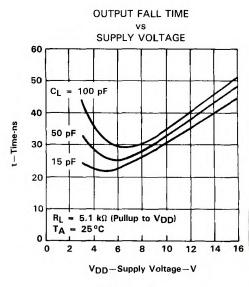


[†]Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

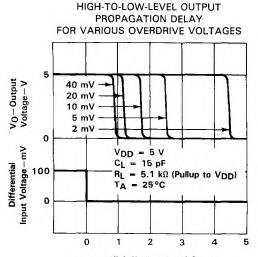




Output Propagation Delay Time - μs

FIGURE 16

FIGURE 17



tp_HL—High-To-Low-Level Output Propagation Delay Time—μs

FIGURE 18

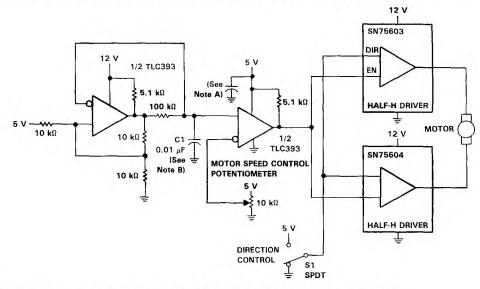


TYPICAL APPLICATION DATA

The input should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less then 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25 °C with VDD = 5 V, both inputs must remain between -0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 µF) positioned as close to the device as possible.

The TLC393 has internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

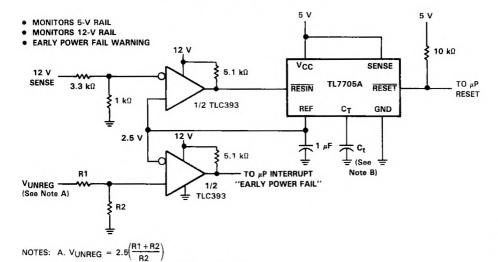


NOTES: A. The recommended minimum capacitance is 10 µF to eliminate common ground switching noise.

B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA



B. The value of C_t determines the time delay of reset.

FIGURE 20. ENHANCED SUPPLY SUPERVISOR

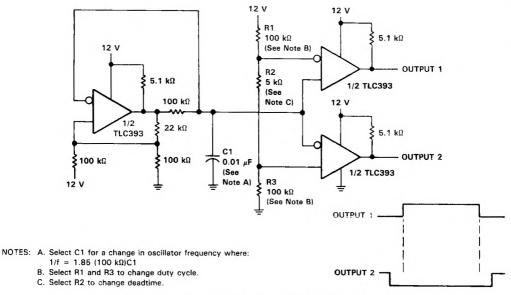


FIGURE 21. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR



TLC3702M, TLC3702I, TLC3702C DUAL MICROPOWER LINCMOS™ COMPARATORS

D3209, NOVEMBER 1986 - REVISED JANUARY 1989

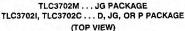
- Push-Pull CMOS Output Drives Capacitive Loads without Pull-Up Resistor,
 IO = ±8 mA
- Very Low Power . . . 100 μW Typ at 5 V
- Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive
- Single Supply Operation:

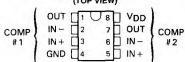
TLC3702M . . . 4 V to 16 V TLC3702I . . . 3 V to 16 V TLC3702C . . . 3 V to 16 V

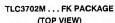
- High Input Impedance . . . 10¹² Ω Typ
- Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days
- On-Chip ESD Protection

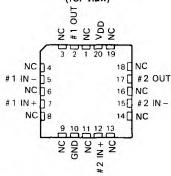
description

The TLC3702 consists of two independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The pushpull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.



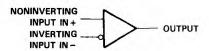






NC-No internal connection

symbol (each comparator)



AVAILABLE OPTIONS

PACKAGE					
TA	V _{IO} max at 25°C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC3702CD		TLC3702CJG	TLC3702CP
-40°C to 85°C	5 mV	TLC3702ID	-	TLC3702IJG	TLC3702IP
-55°C to 125°C	5 mV	=	TLC3702MFK	TLC3702MJG	=

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., TL3702CDR)

LinCMOS is a trademark of Texas Instruments Incorporated.

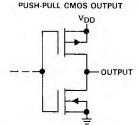


description (continued)

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3702M is characterized for operation over the full military temperature range of -55° C to 125°C. The TLC3702I is characterized for operation over the extended industrial temperature range of -40° C to 85°C. The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)		0.3 V to 18 V
Output voltage, VO		0.3 V to VDD
Input current, II		±5 mA
Output current, IO (each output)		±20 mA
Total supply current into VDD termina		40 mA
Total current out of ground terminal		40 mA
Continuous total dissination	Se	e Dissination Rating Table
Continuous total dissipation		o biooipanon naming rabio
	TLC3702M	55°C to 125°C
	TLC3702M	-55°C to 125°C -40°C to 85°C
Operating free-air temperature range:	TLC3702M	55°C to 125°C 40°C to 85°C 0°C to 70°C
Operating free-air temperature range: Storage temperature range	TLC3702M	55°C to 125°C 40°C to 85°C 0°C to 70°C 65°C to 150°C
Operating free-air temperature range: Storage temperature range Case temperature for 60 seconds: FI	TLC3702M	
Operating free-air temperature range: Storage temperature range	TLC3702M	-55°C to 125°C -40°C to 85°C 0°C to 70°C -65°C to 150°C 260°C 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	- FOWER HATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (TLC3702M)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	528 mW	429 mW	-
P	1000 mW	8.0 mW/°C	640 mW	520 mW	_



TLC3702M DUAL MICROPOWER LINCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM MA	X UNI
Supply voltage, אַרַר	4	5 1	6 V
Common-mode · . · voltage, V _{IC}	0	V _{DD} -	-1.5 V
High-level output current, IOH		-2	0 mA
Low-level output current, IOL		2	20 mA
Operating free-air temperature, TA	-55	12	25 °C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDIT	rionst	MIN	TYP	MAX	UNIT
		V _{IC} = V _{ICR} min,	25°C		1.2	5	
ViO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	-55°C to 125°C			10	mV
l. a	Input offset current	V _{IC} = 2.5 V	25°C		1		pΑ
lo	input onset current	VIC = 2.5 V	125°C			15	nA
b	Input bias current	V _{IC} = 2.5 V	25°C		5		pΑ
ΙΒ	input bias current	VIC = 2.5 V	125°C			30	nA
VICR	Common-mode input		25°C	0 to V _{DD} -1			V
	voltage range		-55°C to 125°C	0 to V _{DD} -1.5			
			25°C		84		
CMRR	Common-mode rejection ratio	VIC = VICRMIN	125°C		83		dB
			−55°C		82		
			25°C		85		
KSVR	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	125°C		85		dB
			−55°C		82		
Vall	High-level output voltage	$V_{ID} = 1 V$	25°C	4.5	4.7		V
VOH	riigii-level obtput voltage	$I_{OH} = -4 \text{ mA}$	125°C	4.2			
Vo	Low-level output voltage	$V_{\text{ID}} = -1 V_{\text{i}}$	25°C		210	300	mV
VOL	LOW-level Output Voltage	IOL = 4 mA	125°C			500	111.0
Inn	Supply current	No load, Outputs low	25°C		18	40	40 μA
IDD	(both comparators)	140 load, Outputs low	-55°C to 125°C	90		μ.	

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

DUAL MICROPOWER LINCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage VDD	3	5	16	٧
Commor · · · nput · · · , V _{IC}	-0.2		V _{DD} -1.5	٧
High-lever output current, 10H			-20	mA
Low-level output current, IOL		2000	20	mA
Operating free-air temperature, TA	-40		85	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDIT	ionst	MIN	TYP	MAX	UNIT	
		V _{IC} = V _{ICR} min,			1.2	5		
۷iO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	-40°C to 85°C			7	mV	
lio.	Input offset current	V _{IC} = 2.5 V	25°C		1		pΑ	
lo	input onset current	VIC = 2.5 V	85°C			1	nA	
lın.	Input bias current	V _{IC} = 2.5 V	25°C	10.00	5		pA	
lΒ	input bias current	VIC - 2.5 V	85°C			2	nA	
V	Common-mode input		25°C	0 to V _{DD} -1			٧	
VICR	voltage range		-40°C to 85°C	0 to V _{DD} -1.5				
			25°C		84			
CMRR	Common-mode rejection ratio	VIC = VICRMIN	85°C		84		dB	
			-40°C		83			
			25°C		85			
KSVR	VR Supply voltage rejection ratio VDD = 5 V	V _{DD} = 5 V to 10 V	85°C		85		dB	
			-40°C		83			
Vон	High-level output voltage	$V_{ID} = 1 V$,	25°C	4.5	4.7		٧	
VOH	riigii-ievel ootput voltage	IOH = -4 mA	85°C	4.3		72.50	V	
Vol	Low-level output voltage	$V_{ID} = -1 V$	25°C		210	300	mV	
*UL	Low-level output voltage	IOL = 4 mA	85°C			400	HIV	
loo	Supply current	No load, Outputs low	25°C		18	40		
DD	(both comparators)	No load, Outputs low	-40°C to 85°C			65	μΑ	

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

TLC3702C DUAL MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3	5	16	٧
Common-mode input voltage, VIC	-0.2		V _{DD} 1.5	٧
High-level output current, IOH			-20	mA
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics at specified operating free-air temperature, $V_{DD} = 5 \text{ V}$ (unless otherwise noted)

	PARAMETER	TEST CONDITION	ons†	MIN	TYP	MAX	UNIT	
		VIC = VICRMIN,	25°C		1.2	5		
VIO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	0°C to 70°C			6.5	mV	
l.a	Input offset current	V _{IC} = 2.5 V	25°C		1		pA	
10	input onset current	VIC - 2.5 V	70°C			0.3	nA	
l	Input bias current	V _{IC} = 2.5 V	25°C		5		pΑ	
lB .	input bias current	VIC = 2.5 V	70°C			0.6	nA	
V	Common-mode input		25°C	0 to V _{DD} -1			V	
VICR	voltage range		0°C to 70°C	0 to V _{DD} -1.5	La con			
17.45			25°C		84			
CMRR	Common-mode rejection ratio	Common-mode rejection ratio	VIC = VICRMIN	70°C	la a se	84		dB
			0°C		84			
			25°C		85			
ksv R	Supply voltage rejection ratio	V _{DD} = 5 V to 10 V	70°C		85		dB	
			0°C	10	85		1	
W	High-level output voltage	V _{ID} = 1 V,	25°C	4.5	4.7		v	
VOH	High-level output voltage	IOH = -4 mA	70°C	4.3				
V	Law level autout valtage	$V_{1D} = -1 V$,	25°C		210	300	mV	
VOL	Low-level output voltage	I _{OL} = 4 mA	70°C			375	inv	
	Supply current		25°C		18	40		
DD D	(both comparators)	No load, Outputs low	0°C to 70°C			50	μΑ	

[†] All characteristics are measured with zero common-mode voltage unless otherwise noted.

TLC3702M, TLC3702I, TLC3702C DUAL MICROPOWER LinCMOS™ COMPARATORS

switching characteristics, $V_{DD} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TES	T CONDITIONS	MIN TYP MAX	UNIT
			Overdrive = 2 mV	4.5	
			Overdrive = 5 mV	2.7	1
•	Propagation delay time, low-to-high-level output	f = 10 kHz,	Overdrive = 10 mV	1.9	1
^t PLH	Propagation delay time, low-to-high-level output	C _L = 50 pF	Overdrive = 20 mV	1.4	μs
			Overdrive = 40 mV	1.1	1
		V _I = 1.4 V ste	p at IN+ pin	1.1	
	Propagation delay time, high-to-low-level output		Overdrive = 2 mV	4.0	
			Overdrive = 5 mV	2.3	μs
		f = 10 kHz, C _L = 50 pF	Overdrive = 10 mV	1.5	
^t PHL			Overdrive = 20 mV	0.95	
			Overdrive = 40 mV	0.65	1
		V _I = 1.4 V step at IN+ pin		0.15	1
**	Fall time	f = 10 kHz,	Overdrive = 50 mV	50	
tf	raii time	CL = 50 pF	Overdrive = 50 mV	50	ns
	Dina tima	f = 10 kHz,	Overdrive - 50 mV	105	
tŗ	Rise time	Cլ = 50 pF	Overdrive = 50 mV	125	ns



Very Low Power . . . 200 μW Typ at 5 V

 Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive

Single Supply Operation:

TLC3704M . . . 4 V to 16 V TLC3704I . . . 3 V to 16 V TLC3704C . . . 3 V to 16 V

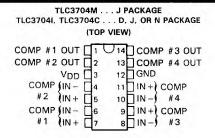
High Input Impedance . . . 10¹² Ω Typ

 Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days

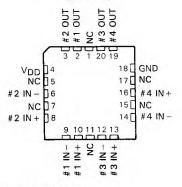
On-Chip ESD Protection

description

The TLC3704 consists of four independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.



TLC3704M . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

AVAILABLE OPTIONS

			PACKA	GE	
TA	V _{IO} max at 25 °C	SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC3704CD		TLC3704CJ	TLC3704CN
-40°C to 85°C	5 mV	TLC3704ID	-	TLC3704IJ	TLC3704IN
- 55°C to 125°C	5 mV		TLC3704MFK	TLC3704MJ	-

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., TLC3704CDR)

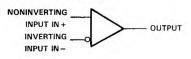
LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

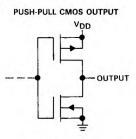
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704M is characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 $^{\circ}$ C. The TLC3704I is characterized for operation over the extended industrial temperature range of $-40\,^{\circ}$ C to 85 $^{\circ}$ C. The TLC3704C is characterized for operation over the commercial temperature range of 0 $^{\circ}$ C to 70 $^{\circ}$ C.

symbol (each comparator)



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VDD (see Note 1)0.3 to 18 V
Differential input voltage (see Note 2)
Input voltage, VI
Output voltage, VO0.3 V to Vpp
Input current, II
Output current, IO (each output) ±20 mA
Total supply current into V _{DD} terminal
Total current out of ground terminal
Continuous total dissipation See Dissipation Rating Table
Operating free-air temperature range: TLC3704M55°C to 125°C
TLC3704I40°C to 85°C
TLC3704C 0°C to 70°C
Storage temperature range
Case temperature for 60 seconds: FK package
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package 300 °C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.

2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE TA = 25°C	TA = 70°C POWER RATING	TA = 85°C POWER RATING	TA = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC3704M)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (All others)	1025 mW	8.2 mW/°C	656 mW	533 mW	_
N	1150 mW	9.2 mW/°C	736 mW	598 mW	_



TLC3704M QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	4	5	16	٧
Common-mode input voltage, V _{IC}	0		V _{DD} – 1.5	٧
High-level output current, IOH			-20	mA
Low-level output current, IOL		Vi.	20	mA
Operating free-air temperature, TA	- 55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDI	TIONS†	MIN	TYP	MAX	UNIT
		VIC = VICRMIN,	25°C		1.2	5	
VIO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	-55°C to 125°C			10	mV
h	Input offset current	V 2 E V	25 °C		1		pA
10		V _{IC} = 2.5 V	125°C			15	nA
1.2	Inches bing property	V 2 F V	25°C		5		pΑ
IB	Input bias current	$V_{IC} = 2.5 V$	1. C			30	nA
			25°C	0 to V _{DD} - 1		-41	
VICR	Common-mode input voltage range		-55°C to 125°C	0 to V _{DD} – 1.5			1,
	Common-mode rejection ratio	V _{IC} = V _{ICR} min	25°C		84		
CMRR			125°C		83		dB
			-55°C		82		
			25°C		85		
ksvr	Supply voltage rejection ratio	$V_{DD} = 5 V \text{ to } 10 V$	·. c		85		dB
			JL C		82		
	I E - b I I	V _{ID} = 1 V,	25°C	4.5	4.7		V
VOH	High-level output voltage	$I_{OH} = -4 \text{ mA}$	125°C	4.2			1 °
17-	1 11	$V_{ID} = -1 V$	25°C		210	300	
VOL	Low-level output voltage	$I_{OL} = 4 \text{ mA}$	125°C			500	m∨
	S	No load,	25°C		35	80	J. W.
DD	Supply current (four comparators)	Outputs low	-55°C to 125°C			175	μА

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3	5	16	٧
Common-mode input voltage, VIC	-0.2		V _{DD} - 1.5	٧
High-level output current, IOH			-20	mA
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	-40		85	°C

electrical characteristics at specified operating free-air temperature, VDD = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDI	rions†	MIN	TYP	MAX	UNIT
	V _{IC} = V _{ICR} min,		25 °C		1.2	5	
Vio	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	-40°C to 85°C				mV
L. S.	l	V 2.F.V	25 °C		1	- 1	pΑ
10	Input offset current	$V_{IC} = 2.5 V$	85°C			5 7	nA
i		V 25V	25 °C		5		pA
IB	Input bias current	$V_{IC} = 2.5 V$	85 °C			2	nA
14			25°C	0 to V _{DD} – 1			v
VICR	Common-mode input voltage range		-40°C to 85°C	0 to V _{DD} - 1.5			V
	Common-mode rejection ratio		25 °C		84		
CMRR		V _{IC} = V _{ICR} min	85°C		84		₫B
			-40°C		83		
			25°C	3	85		
ksvr	Supply voltage rejection ratio	$V_{DD} = 5 V to 10 V$	85°C		85		dB
	Assert of the second se		-40°C	Land of the same	83		
V	High level autout valtage	$V_{ID} = 1 V_{r}$	25°C	4.5	4.7		V
VOH	High-level output voltage	$1_{OH} = -4 \text{ mA}$	85 °C	4.3		- 7	V
·/	Law level output veltore	$V_{ID} = -1 V$,	25 °C		210		mV
VOL	Low-level output voltage	IOL = 4 mA	85 °C				mv
1	Supply gurrant (faur comparators)	No load,	25 °C		35	80	
DD	Supply current (four comparators)	Outputs low	-40°C to 85°C			125	μА

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted. NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.



TLC3704C QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{DD}	3	5	16	٧
Common-mode input voltage, VIC	-0.2		V _{DD} - 1.5	٧
High-level output current, IOH			-20	mA
Low-level output current, IOL			20	mA
Operating free-air temperature, TA	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDIT	TIONS†	MIN	TYP	MAX	UNIT
		V _{IC} = V _{ICR} min,	25°C		1.2	5	
VIO	Input offset voltage	V _{DD} = 5 V to 10 V, See Note 3	0°C to 70°C			6.5	m∨
	1	V 0 E V	25 °C		1		pΑ
10	Input offset current	$V_{IC} = 2.5 V$	70°C			0.3	nA
i.	1	V . 25 V	25°C		5		pA
IB	Input bias current	$V_{IC} = 2.5 V$	70°C			0.6	nA
			25°C	0 to V _{DD} - 1			
VICR	Common-mode input voltage range		0°C to 70°C	0 to V _{DD} - 1.5			٧
	Common-mode rejection ratio	VIC = VICRMIN	25 °C		84		
CMRR			70°C		84		dB
			0°C		84		
			25°C		85		
KSVR	Supply voltage rejection ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V}$	70°C		85		dΒ
			0°C	YP THE TAX	85		
	Ol-t I	V _{ID} = 1 V,	25°C	4.5	4.7		V
∨он	High-level output voltage	$I_{OH} = -4 \text{ mA}$	70°C	4.3			V
	1 1 1 1	$V_{ID} = -1 V$,	25°C		210		
VOL	Low-level output voltage	IOL = 4 mA	70°C				mV
	S (fa	No load,	25°C		35	80	
ססי	Supply current (four comparators)	Outputs low	0°C to 70°C			100	μА

[†]All characteristics are measured with zero common-mode voltage unless otherwise noted.

TLC3704M, TLC3704I, TLC3704C QUADRUPLE MICROPOWER LinCMOS™ COMPARATORS

switching characteristics, VDD = 5 V, TA = 25 °C

	PARAMETER	TEST	CONDITIONS	MIN TYP	MAX	UNIT
			Overdrive = 2 mV	4.5		
	Propagation delay time, low-to-high-level output	4 10 111-	Overdrive = 5 mV	2.7		
		f = 10 kHz,	Overdrive = 10 mV	1.9		
[†] PLH		C _L = 50 pF	Overdrive = 20 mV	1.4		μS
			Overdrive = 40 mV	1.1		1
		V _I = 1.4-V step	at IN+ pin	1.1	4-5-81	
	Propagation delay time, high-to-low-level output		Overdrive = 2 mV	4.0		
		(10 111-	Overdrive = 5 mV	2.3		7
		f = 10 kHz,	Overdrive = 10 mV	1.5		1
TPHL		C _L = 50 pF	Overdrive = 20 mV	0.95		μS
			Overdrive = 40 mV	0.65]
		V _I = 1.4-V ster	p at IN+ pin	0.15		
	F-0 single bight to love board and and	f = 10 kHz,	Overdrive = 50 mV			
tf	Fall time, high-to-low-level output	CL = 50 pF	Overdrive = 50 mv	50		กร
	Rise time, low-to-high-level output	f = 10 kHz	Overdrive = 50 mV	105		
t _r		C _L = 50 pF	Overdive = 50 mV	125		ns

